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PACKAGING HANDBOOK

1991

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Introduction

1

1



CHAPTER 1 INTRODUCTION

OVERVIEW OF INTEL PACKAGING TECHNOLOGY

As semiconductor devices become significantly more complex, electronics designers are challenged to fully harness their computing power. Today's products can feature more than one million transistors, and device count is expected to increase more than a hundredfold by the year 2000. With a greater number of functions integrated on a die or chip of silicon, manufacturers and users will face new and increasingly challenging electrical interconnect issues. To tap the power of the die efficiently, each level of electrical interconnect from the die to the functional hardware or equipment must also keep pace with these revolutionary devices. Package design, at the first interconnect level, has a major impact on device performance and functionality.

1

Today, submicron feature size at the die level are driving package feature size down to the design-rule level of the early transistors. At the same time, electronic equipment designers are shrinking their products, increasing complexity, and setting higher expectations for performance. To meet these demands, package technology must deliver higher lead counts, reduced pitch, minimum footprint area, and significant overall volume reduction.

Circuit performance is only as good as the weakest link. Therefore, device performance is for all practical purposes determined by the package. While packaging cannot add to the theoretical performance of the device design, it can have adverse effects if not optimized. An optimum package design would achieve 100% of the theoretical device, application-specific performance, which in practice is un-achievable. Package performance, therefore, is the best compromise of electrical, thermal, and mechanical attributes, as well as physical outline, to meet product specific reliability and cost objectives.

These factors have driven a variety of major innovations in Intel package design, such as surface mount, small out-line, and very thin packages. The introduction of additional advanced Intel packaging technologies to evolving needs will continue aggressively throughout the 1990s. For example, in 1990, Intel introduced the multilayer molded plastic quad flatpack (MM-PQFP) and Land Grid Array (LGA). The MM-PQFP, Intel's patented concept, enhances the electrical performance of the molded lead frame package by incorporating isolated ground and power planes within the assembly. After molding, the multilayer construction is totally embedded in the molded body and is not evident on the outside. The LGA is a new package/socket concept for semiconductor devices that uses a standard multilayer, co-fired ceramic package in conjunction with several unique board-level, Z-direction interconnect, low-profile sockets.

Among the new packages now on the drawing board, with introductions planned for 1992, is the high-density plastic quad flatpack (HD-PQFP). This package, featuring a unique film-embedded perimeter lead concept, is targeted for applications requiring plastic packages with more than 200 I/Os.

Fit, form, and function are in the eye of the beholder, and any Intel device can serve more than one market and/or application requiring widely divergent package attributes.

Therefore, “one size fits all” is not a practical approach to device packaging. Packaging technology is not a single technology, but instead consists of more than 20 industry proven combinations of technologies or technology sets that can be categorized by package families. In support of the growing number of Intel devices and to meet the industry demand for package-specific applications, Intel’s package portfolio has more than doubled during the last eight years.

PURPOSE OF THIS HANDBOOK

Intel’s Packaging Handbook is intended to serve as a data reference for engineering design, as well as a guide to Intel package selection and availability. Each of the eight chapters provides a comprehensive and in-depth analysis of Intel packaging technology, from information on IC assembly, performance characteristics, and physical constants, to detailed discussions of surface mount technology and Intel shipping and packing.

Chapter 1 provides an analysis of Intel’s package families, including package attributes, package types, and a package selection guide. (CD-ROM Literature Order Number: 240817-001)

Chapter 2 offers a detailed view into Intel package module outlines and dimensions. (CD-ROM Literature Order Number: 231369-007)

Chapter 3 covers assembly manufacturing technology. The chapter begins with a brief introduction and a discussion of statistical tools used in the manufacturing process. It also includes a comprehensive analysis of Intel’s IC assembly process flow. (CD-ROM Literature Order Number: 240818-001)

Chapter 4 explores package characteristics and tabulates in-depth data of electrical, mechanical, and thermal IC package characteristics. (CD-ROM Literature Order Number: 240819-001)

Chapter 5 addresses physical constants of IC package materials. The charts in this chapter provide valuable information on mechanical, electrical, and thermal properties of case materials, lead/lead frames, and soldering material characteristics. (CD-ROM Literature Order Number: 240820-001)

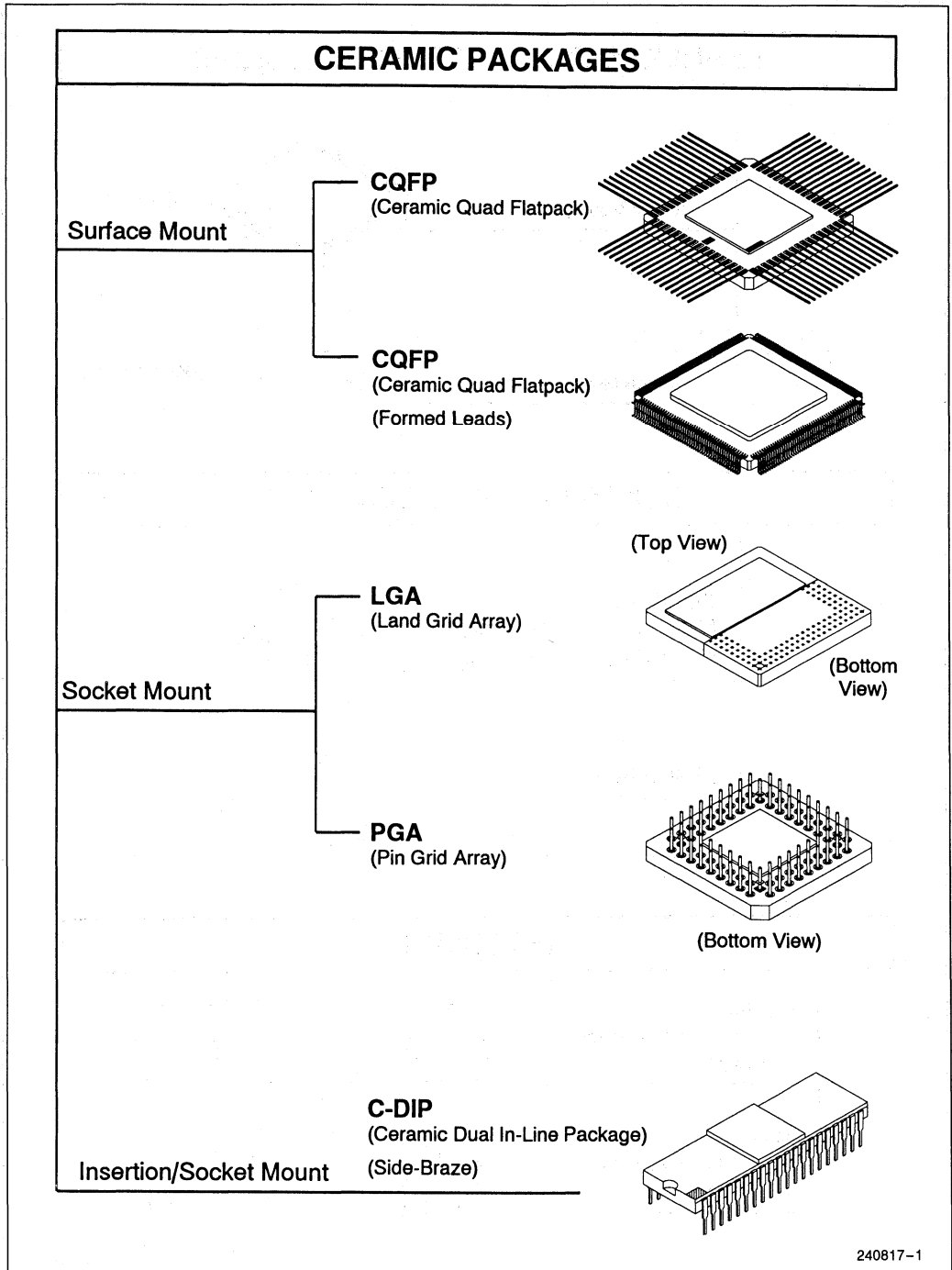
Chapter 6 explores surface mount technology, desiccant pack, and board removal techniques. (CD-ROM Literature Order Number: 240821-001)

Chapter 7 describes the various packing and shipping methods used at Intel. Packing media, desiccant pack materials, and shipping data are clearly illustrated. (CD-ROM Literature Order Number: 240822-001)

Chapter 8 provides the reader with a listing of international packaging specifications and a comprehensive resource library. (CD-ROM Literature Order Number: 240829-001)

Glossary offers a detailed view of packaging related technical terminology. (CD-ROM Literature Order Number: 240823-001)

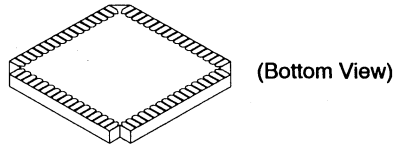
PACKAGE TYPES



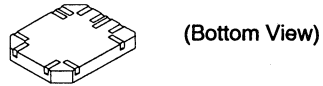
PACKAGE TYPES (Continued)

LEADLESS CHIP CARRIER PACKAGES

LCC
(Socket Mount)

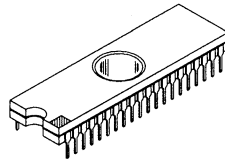


LCC
(Surface Mount)

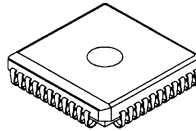


GLASS-SEALED PACKAGES

CERDIP
(Ceramic Dual In-Line Package)
(Insertion Mount; UV Window)

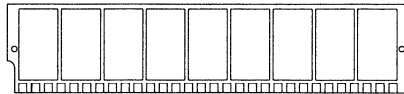


CERQUAD
(Ceramic Quadpack)
(Surface Mount)



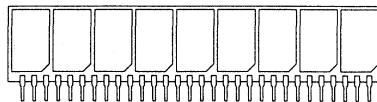
MODULES

SIMM
(Single In-Line Leadless
Memory Module)



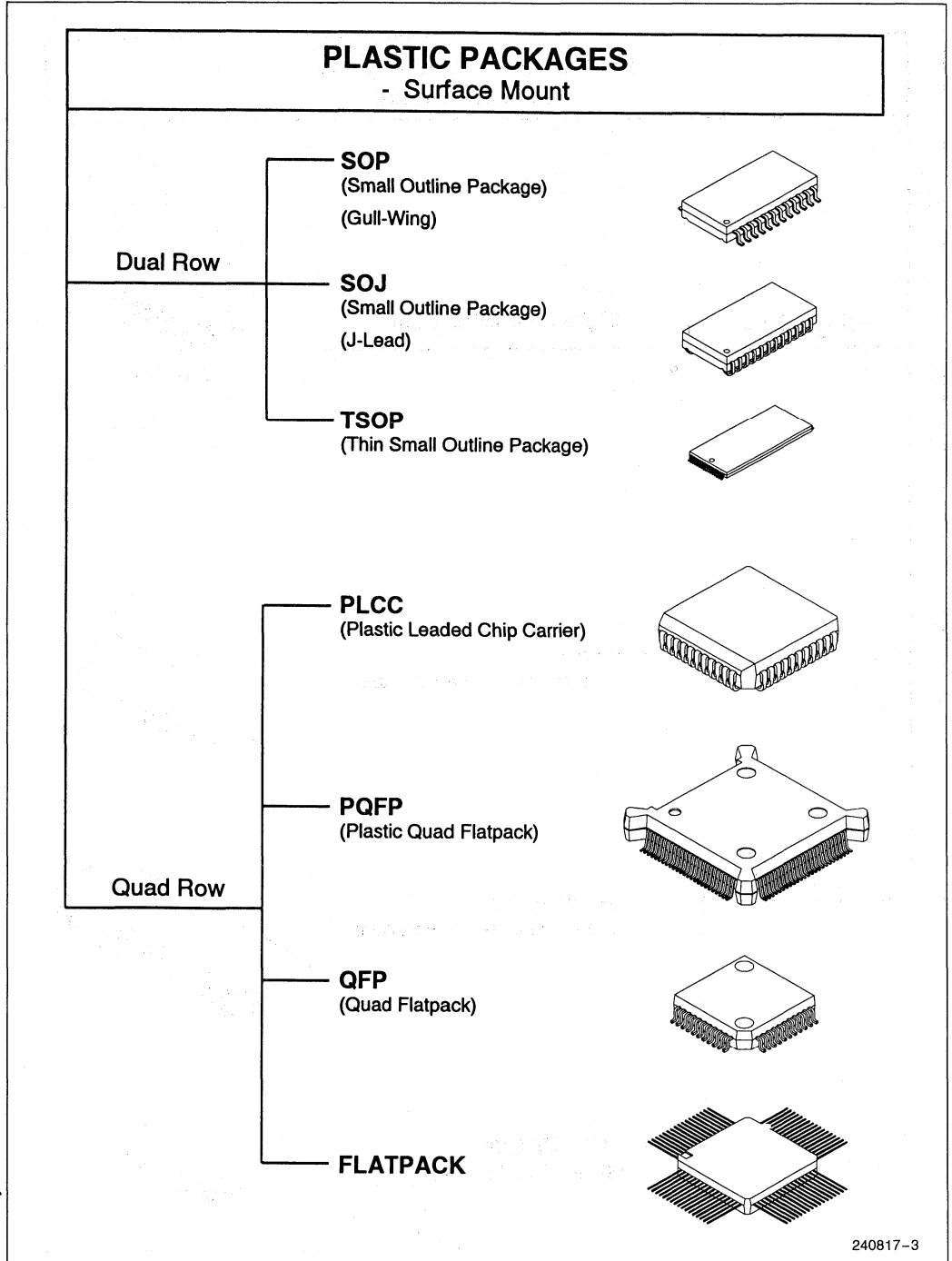
(Top View)

SIP
(Single In-Line Leaded
Memory Module)



(Top View)

PACKAGE TYPES (Continued)



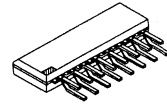
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PACKAGE TYPES (Continued)

PLASTIC PACKAGES
- Insertion Mount

Single Row

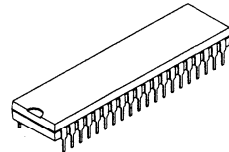
ZIP
(ZigZag In-Line Package)



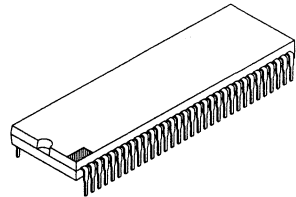
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Dual Row

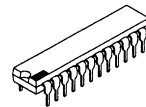
P-DIP
(Plastic Dual In-Line Package)



SHRINK DIP
(Shrink Dual In-Line Package)



SKINNY DIP
(Skinny Dual In-Line Package)



240817-4

CERAMIC PACKAGE ATTRIBUTES

Ceramic Dual In-Line Package (C-DIP)								
Lead Count	16	18	22	24	28	32	40	48
Sq./Rect.	R	R	R	R	R	R	R	R
Pitch (inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.109	0.109	0.109	*0.130 0.100	*0.132 0.102	0.120	*0.154 0.123	*0.172 0.142
Weight (gm)								
Max. Footprint (inches)								
UV Eraseable				X	X	X	X	X
Shipping Media Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X
Desiccant Package								
Comments/ Footnotes	*EPROM Lid							

1

Ceramic Land Grid Array			
Lead Count	144	168	227
Sq./Rect.	S	S	S
Pitch (inches)	0.050	0.100	0.050
Package Thickness (inches)	0.113	0.125	0.113
Weight (gm)	4.0		4.0
Max. Footprint Cavity Up/Down	Up	Down	Up
UV Eraseable			
Shipping Media: Tubes Tape & Reel Trays	X	X	X
Desiccant Pack			
Comments/ Footnotes			



CERAMIC PACKAGE ATTRIBUTES (Continued)

Leadless Chip Carrier (LCC)							
Lead Count	18	20	28	32	44	68	68
Sq./Rect.	R	R	S	R	S	S	S
Pitch (inches)	0.050	0.050	0.050	0.050	0.050	0.050	0.050
Package Thickness (inches)	0.068	0.068	0.073	*0.080 0.108	*0.092 0.120	0.096	0.130
Weight (gm)							
Max. Footprint (inches)							
UV Eraseable	X	X	X	See Note	See Note		X
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X
Desiccant Pack							
Comments/ Footnotes	32L— 0.080 = Solid Lid, Non-UV. 32L— 0.108 = EPROM Lid, UV. 44L— 0.092 = Solid Lid, Non-UV. 44L— 0.120 = EPROM Lid, UV.						

Pin Grid Array (PGA)										
Lead Count	68	68	68	88	88	88	132	168	208	240–280
Sq./Rect.	S	S	*S	S	S	*S	S	S	S	S
Pitch (inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.105	0.110	0.125	0.105	0.110	0.125	0.110	0.110	0.110	0.110
Weight (Gm)										
Max. Footprint (inches)	1.15	1.15	1.15	1.35	1.35	1.35	1.450	1.750	1.750	1.950
UV Eraseable			X			X				
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X	X	X
Desiccant Pack										
Comments/ Footnotes	*With EPROM									

CERAMIC PACKAGE ATTRIBUTES (Continued)

Ceramic Quad Flatpack (CQFP)			
Lead Count	68	164	196
Sq./Rect.	S	S	S
Pitch (inches)	0.050	0.025	0.025
Package Thickness (inches)			
Weight (gm)	12	12	17
Max. Footprint (inches)			
UV Eraseable	X		
Shipping Media: Carrier Tape & Reel Trays	X	X	X X
Desiccant Pack			
Comments/ Footnotes	196L is also Available with Formed Leads (Shipped in Trays)		

1

CERDIP									
Lead Count	16	18	20	22	24	28	32	40	42
Sq./Rect.									
Pitch (mm)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.157	0.157	0.153	0.165	0.165	0.167	0.167	0.167	0.167
Weight (gm)					1.69				
Max. Footprint (inches)									
UV Eraseable	X	X	X	X	X	X	X	X	X
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X	X
Desiccant Pack									
Comments/ Footnotes	Available with or without UV Window								

CERAMIC PACKAGE ATTRIBUTES (Continued)

Ceramic QuadPack (CERQUAD)			
Lead Count	44	52	68
Sq./Rect.	S	S	S
Pitch (inches)	0.050	0.050	0.050
Package Thickness (inches)	0.172	0.172	0.172
Weight (gm)	2.85	3.59	7.14
Max. Footprint (inches)	0.72	0.82	1.02
UV Eraseable	X	X	X
Shipping Media: Tubes Tape & Reel Trays	X	X	X
Desiccant Pack			
Comments/ Footnotes	Available with or without UV Window		

PLASTIC PACKAGE ATTRIBUTES

Plastic Dual In-Line (PDIP)									
Lead Count	16	18	20	24	28	32	40	48	64
Sq./Rect.	R	R	R	R	R	R	R	R	R
Pitch (inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.132	0.132	0.132	0.152	0.152	0.150	0.160	0.162	0.167
Weight (gm)	1.045	1.248	1.418			4.815	6.128	7.912	
Max. Footprint (inches)									
UV Eraseable									
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X	X	X	X
Desiccant Pack									
Comments/ Footnotes	Some pin counts available in; Halflead, Widebody; Widebody; and Standard Type P.								

PLASTIC PACKAGE ATTRIBUTES (Continued)

Plastic (Flatpack)	
Lead Count	68
Sq./Rect.	S
Pitch (inches)	0.050
Package Thickness (inches)	0.168
Weight (gm)	
Max. Footprint (inches)	
UV Eraseable	
Shipping Media: Tubes Tape & Reel Carrier	X
Desiccant Pack	
Comments/ Footnotes	Through Hole Use Only

1

Plastic Quad Flatpack (PQFP)						
Lead Count	68	84	100	132	164	196
Sq./Rect.	S	S	S	S	S	S
Pitch (inches)	0.025	0.025	0.025	0.025	0.025	0.025
Package Thickness (inches)	0.170	0.170	0.170	0.170	0.170	0.170
Weight (gm)			2.8	4.2	6.1	
Max. Footprint (inches)						
UV Eraseable						
Shipping Media:						
Tubes	X	X	X	X	X	X
Tape & Reel	X	X	X	X	X	X
Trays	X	X	X	X	X	X
Desiccant Pack	X	X	X	X	X	X
Comments/ Footnotes	All PQFPs are "Gull Wing" with bumpers					

PLASTIC PACKAGE ATTRIBUTES (Continued)

Quad Flatpack (QFP)						
Lead Count	44	48	64	80	80	208
Sq./Rect.	S	S	S	S	R	S
Pitch (mm)	0.800	0.500	0.650	0.500	0.800	0.500
Package Thickness (inches)	0.096	0.065	0.100	0.065	0.114	0.140
Weight (gm)						
Max. Footprint (inches)						
UV Eraseable						
Shipping Media: Tubes Tape & Reel Trays	X	X	X	X	X	X
Desiccant Pack						
Comments/ Footnotes	Gull Wing Lead Configuration, non-bumpered					

Plastic Leaded Chip Carrier (PLCC)								
Lead Count	20	28	28	32	44	52	68	84
Sq./Rect.	S	S	R	R	S	S	S	S
Pitch (inches)	0.050	0.050	0.050	0.050	0.050	0.050	0.050	0.050
Package Thickness (inches)	0.152	0.152	0.108	0.108	0.148	0.150	0.150	0.150
Weight (gm)	0.705	1.15	0.85	1.1	2.31	3.17	4.8	6.2
Max. Footprint (inches)	0.390	0.490	See Note	See Note	0.690	0.790	0.990	0.190
UV Eraseable								
Shipping Media: Tubes Tape & Reel Trays	X X X	X X X	X X X	X X X	X X X	X	X X X	X X X
Desiccant Pack	X	X	X	X	X	X	X	X
Comments/ Footnotes	All PLCC's are "J" Lead 28R—0.39 x 0.59 32R—0.49 x 0.59							

PLASTIC PACKAGE ATTRIBUTES (Continued)

Small Outline Package (SOJ)		
Lead Count	20	24
Sq./Rect.	R	R
Pitch (mm)	1.27	1.27
Package Thickness (Inches)	0.105	0.113
Weight (gm)		
Max. Footprint Inches	0.300	0.300
UV Eraseable		
Shipping Media:		
Tubes	X	X
Tape & Reel	X	X
Trays		
Desiccant Pack	X	X
Comments/ Footnotes	"J" Lead Configuration	

1

Small Outline Package (SOP)	
Lead Count	28
Sq./Rect.	R
Pitch (mm)	1.27
Package Thickness (inches)	0.108
Weight (gm)	0.70
Max. Footprint (inches)	0.330
UV Eraseable	
Shipping Media:	
Tubes	X
Tape & Reel	
Trays	
Desiccant Pack	X
Comments/ Footnotes	Gull Wing Lead Configuration

PLASTIC PACKAGE ATTRIBUTES (Continued)

Thin Small Outline Package (TSOP)	
Lead Count	32
Sq./Rect.	R
Pitch (mm)	0.50
Package Thickness (inches)	1.2
Weight (gm)	0.37
Max. Footprint (inches)	
UV Eraseable	
Shipping Media: Tubes Tape & Reel Trays	X
Desiccant Pack	X
Comments/ Footnotes	TSOP is "Gull Wing" Configuration

Zig-Zag In-Line Package (ZIP)		
Lead Count	16	20
Sq./Rect.	R	R
Pitch (mm)	1.27	1.27
Package Thickness (inches)	0.115	0.118
Weight (gm)		
Max. Footprint (inches)		
UV Eraseable		
Shipping Media: Tubes Tape & Reel Trays	X	X
Desiccant Pack		
Comments/ Footnotes	Zig-Zag Lead Configuration	

MODULE ATTRIBUTES

Single In-Line Leaded Memory Module (SIP)	
Lead Count	30
Sq./Rect.	R
Pitch (mm)	2.54
Package Thickness (inches)	2.00
Weight (gm)	
Max. Footprint (inches)	3.10
UV Eraseable	
Shipping Media: Tubes Tape & Reel Trays	X
Desiccant Pack	
Comments/ Footnotes	Insertable Module

Single In-Line Leadless Memory Module (SIMM)		
Lead Count	30	80
Sq./Rect.	R	R
Pitch (inches)	0.100	0.050
Package Thickness (inches)	0.20	0.33
Weight (gm)		15.7
Max. Footprint (inches)	3.50	4.65
UV Eraseable		
Shipping Media: Tubes Tape & Reel Trays	X	X
Desiccant Pack		
Comments/ Footnotes	JEDEC Standard Insertable Module	

1



PACKAGE/MODULE SELECTION GUIDE

Lead Count	Package Designator	Package Type	Nominal Pitch (inches)	Special Notes
16	C	C-DIP	0.100	
18	C	C-DIP	0.100	
22	C	C-DIP	0.100	
24	C	C-DIP	0.100	
28	C	C-DIP	0.100	
32	C	C-DIP	0.100	
40	C	C-DIP	0.100	
48	C	C-DIP	0.100	
18	R	LCC	0.050	
20	R	LCC	0.050	
28	R	LCC	0.050	
32	R	LCC	0.050	
44	R	LCC	0.050	
68	R	LCC	0.050	
68	R	LCC	0.050	UV Window
68	A	PGA	0.100	
88	A	PGA	0.100	
68	A	PGA	0.100	
88	A	PGA	0.100	Cavity Down
132	A	PGA	0.100	Cavity Down
168	A	PGA	0.100	Cavity Down
208	A	PGA	0.100	Cavity Down
240-280	A	PGA	0.100	Cavity Down
16	D	CERDIP	0.100	
18	D	CERDIP	0.100	
20	D	CERDIP	0.100	
22	D	CERDIP	0.100	
24	D	CERDIP	0.100	
24	D	CERDIP	0.100	Skinny DIP
28	D	CERDIP	0.100	
28	D	CERDIP	0.100	Skinny DIP
32	D	CERDIP	0.100	
40	D	CERDIP	0.100	
42	D	CERDIP	0.100	
44	J	CERQUAD	0.050	
52	J	CERQUAD	0.050	
68	J	CERQUAD	0.050	
68	Q	CQFP	0.050	
164	K	CQFP	0.025	Fine Pitch
196	K	CQFP	0.025	Fine Pitch
196	KK	CQFP	0.025	Fine Pitch



PACKAGING

PACKAGE/MODULE SELECTION GUIDE (Continued)

Lead Count	Package Designator	Package Type	Nominal Pitch (inches)	Special Notes
16	P	PDIP	0.100	
16	P	PDIP	0.100	Widebody
18	P	PDIP	0.100	
18	P	PDIP	0.100	Widebody
18	P	PDIP	0.100	1/2 Lead
20	P	PDIP	0.100	
24	P	PDIP	0.100	
24	P	PDIP	0.100	Skinny DIP
24	P	PDIP	0.100	600 mil
28	P	PDIP	0.100	
28	P	PDIP	0.100	Skinny DIP
28	P	PDIP	0.100	
32	P	PDIP	0.100	
40	P	PDIP	0.100	1/2 Lead
40	P	PDIP	0.100	
48	P	PDIP	0.100	
64	P	PDIP	0.070	Shrink DIP
68	KD	PQFP	0.025	Die Down
68	NG	PQFP	0.025	DD/Heatspreader
84	KD	PQFP	0.025	Die Down
100	KD	PQFP	0.025	Die Down
100	KU	PQFP	0.025	Die Up
100	NG	PQFP	0.025	DD/Heatspreader
132	KD	PQFP	0.025	Die Down
132	KU	PQFP	0.025	Die Up
132	NG	PQFP	0.025	DD/Heatspreader
164	KU	PQFP	0.025	Die Up
196	KU	PQFP	0.025	Die Up
28	N	PLCC	0.050	Rect.
32	N	PLCC	0.050	Rect.
20	N	PLCC	0.050	Sq.
28	N	PLCC	0.050	Sq.
44	N	PLCC	0.050	Sq.
68	N	PLCC	0.050	Sq.
52	N	PLCC	0.050	Sq.
84	N	PLCC	0.050	Sq.
68	FP	P FP	0.050	
144	B	LGA	0.050	
168	B	LGA	0.100	
227	B	LGA	0.050	
30	SM	SIMM	0.100	
80	SM	SIMM	0.100	

1



PACKAGE/MODULE SELECTION GUIDE (Continued)

Lead Count	Package Designator	Package Type	Nominal Pitch (inches)	Special Notes
32	E	TSOP	0.500	Die Up
32	F	TSOP	0.500	Die Down
30	GB	SIP	2.54	
16	Z	ZIP	1.27	
20	Z	ZIP	1.27	
28	PA	SOP	1.27	
20	PE	SOJ	1.27	
24	PE	SOJ	1.27	
44	S	QFP	0.800	Square
48	S	QFP	0.500	Square
64	S	QFP	0.650	Square
80	S	QFP	0.500	Square
80	S	QFP	0.800	Rectangular
208	S	QFP	0.500	

NOTE:

For packages without "Special Notes," contact your local Intel FSE for additional package information and specifications.

Package/Module Outlines and Dimensions

2

2

Package/Module Outlines and Dimensions

Intel Product Identification Codes

NG 8 0 3 8 6 S X 1 6 S X 3 8 7

Up to 15 Alphanumeric Characters
for Device Types

Up to 6 Alphanumeric Characters to
Show Customer Specific requirements

Package Type

- A - Ceramic Pin Grid Array
 - B - Ceramic Land Grid Array
 - C - Ceramic Dual In-Line Package
 - D - Cerdip Dual In-Line Package
 - E - Thin Small Out-Line Package, Die Up
 - F - Thin Small Out-Line Package, Die Down
 - FP - Plastic Flatpack Package
 - GB - Single In-Line Leaded Memory Module
 - J - Cerquad Package
 - K - Ceramic Quad Flatpack Package, Fine Pitch, Flat Leads
 - KD - Plastic Quad Flatpack Package, Fine Pitch, Die Down
 - KK - Ceramic Quad Flatpack Package, Fine Pitch, Formed Leads
 - KU - Plastic Quad Flatpack Package, Fine Pitch, Die Up
 - N - Plastic Leaded Chip Carrier
 - NG - Plastic Quad Flatpack, Fine Pitch, Die Down w/ Heat spreader
 - P - Plastic Dual In-Line Package
 - PA - Small Out-Line "Gull-Wing" Package
 - PE - Small Out-Line "J"-Lead Package
 - Q - Ceramic Quad Flatpack Package
 - R - Ceramic Leadless Chip Carrier
 - S - Quad Flatpack Package
 - SM - Single In-Line Leadless Memory Module
 - X - Unpackaged Devices
 - Z - Zigzag In-Line Package
-
- A - Indicates automotive operating temperature range
 - I - Indicates industrial grade
 - L - Indicates extended operating temperature range (-40°C to +85°C) express product with 160 ± 8 hrs. dynamic burn-in.
 - Q - Indicates commercial temperature range (0°C to 70°C) express product with 160 ± 8 hrs. dynamic burn-in.
 - T - Indicates extended temperature range (-40°C to +85°C) express product without burn-in.

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EXAMPLES:

A80486DX25SX387 32-Bit Microprocessor, 25 MHz, 168-Lead Ceramic Pin Grid Array
 NG80386SX16SX159 16-Bit Microprocessor, 16 MHz, 100-Lead Plastic Quad Flatpack

Package/Module Outlines and Dimensions

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CERAMIC SIDEBRAZE DUAL IN-LINE PACKAGE

Symbol List for Ceramic Side Braze Dual In-Line Family

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
A ₁	Distance between seating plane and base plane
A ₂	Distance from base plane to highest point of body (lid)
A ₃	Base body thickness
B	Width of terminal leads
B ₁	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package dimension of length
D ₂	A body length dimension, end lead center to end lead center
E	Largest overall package width dimension outside of lead
E ₁	Body width dimensions not including leads
e _A	Linear spacing of true minimum lead position center line to center line
e _B	Linear spacing between true lead position outside of lead to outside of lead
e ₁	Linear spacing between centerlines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	The total number of potentially useable lead positions
S	Distance from true position centerline of No. 1 lead position to the extremity of the body
S ₁	Distance from other end lead edge positions to the extremity of the body
α	Angular spacing between minimum and maximum lead positions measured at the gauge plane

2

NOTES:

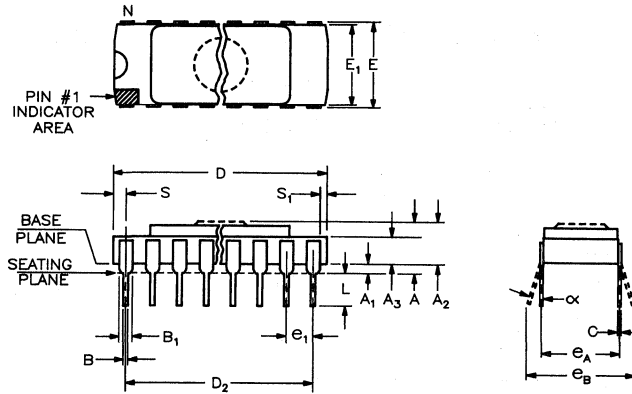
1. Controlling dimension: millimeter.
2. Dimension "e₁" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimension "B₁" is nominal.

Packaging Family Attributes	
Category	Ceramic Dual-In-Line
Acronym	C-DIP or Side Brazed
Lead Configuration	Sidebraze
Lead Counts	16, 18, 22, 24, 32, 40, 48
Lead Finish	Gold Plate
Lead Pitch	0.100"
Board Assembly Type	Socket and Insertion Mount
Standard Registration	JEDEC

NOTES:

1. Alloy 42 or Kovar Leads.
2. Multilayer Co-Fired Ceramic Body.

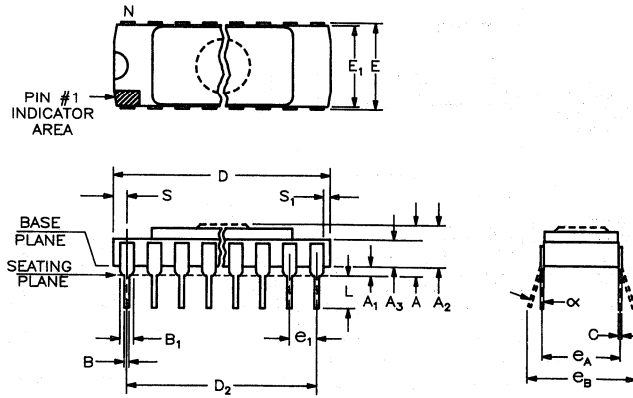
16 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.79	4.32		0.110	0.170	
A ₁	0.64	1.27		0.025	0.050	
A ₂	2.16	3.40		0.085	0.134	
A ₃	1.91	3.05		0.075	0.120	
B	0.38	0.56		0.015	0.022	
B ₁	1.37		Typical	0.054		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	20.07	20.57		0.790	0.810	
D ₂	17.78		Reference	0.700		Reference
E	7.62	8.13		0.300	0.320	
E ₁	7.37	7.62		0.290	0.300	
e ₁	2.29	2.79		0.090	0.110	Typical
e _A	7.37		Reference	0.290		Reference
e _B	7.62	8.38		0.300	0.330	
L	3.18	4.06		0.125	0.160	
N	16			16		
S	0.76	1.78		0.030	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

18 LEAD CERAMIC DUAL IN-LINE PACKAGE

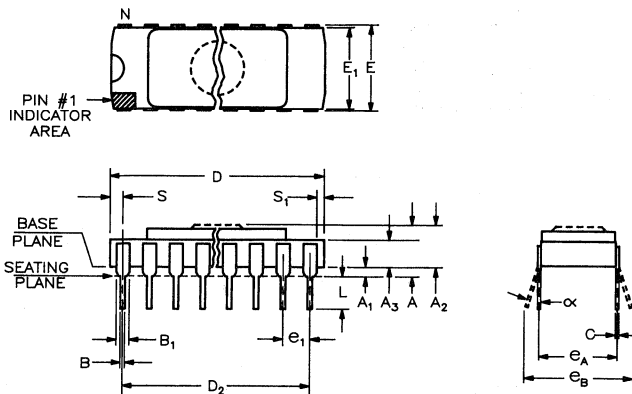


231369-2

2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.79	4.32		0.110	0.170	
A ₁	0.64	1.27		0.025	0.050	
A ₂	2.16	3.40		0.085	0.134	
A ₃	1.91	3.05		0.075	0.120	
B	0.38	0.56		0.015	0.022	
B ₁	1.37		Typical	0.054		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	22.61	23.11		0.890	0.910	
D ₂	20.32		Reference	0.800		Reference
E	7.62	8.13		0.300	0.320	
E ₁	7.37	7.62		0.290	0.300	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.37		Reference	0.290		Reference
e _B	7.62	8.38		0.300	0.330	
L	3.18	4.06		0.125	0.160	
N	18			18		
S	0.76	1.78		0.030	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

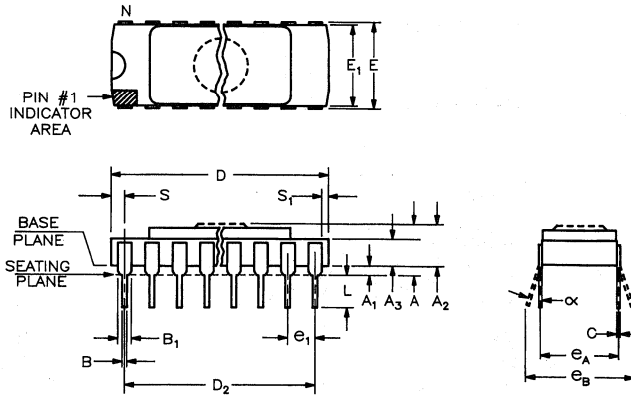
22 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.79	4.32		0.110	0.170	
A ₁	0.64	1.27		0.025	0.050	
A ₂	2.16	3.40		0.085	0.134	
A ₃	2.03	3.05		0.080	0.120	
B	0.38	0.56		0.015	0.022	
B ₁	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	27.56	28.32		1.085	1.115	
D ₂	25.40		Reference	1.000		Reference
E	7.62	8.13		0.300	0.320	
E ₁	7.37	7.62		0.290	0.300	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.37		Reference	0.290		Reference
e _B	7.62	9.14		0.300	0.360	
L	3.18	4.06		0.125	0.160	
N	22			22		
S	0.76	1.78		0.030	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

24 LEAD CERAMIC DUAL IN-LINE PACKAGE

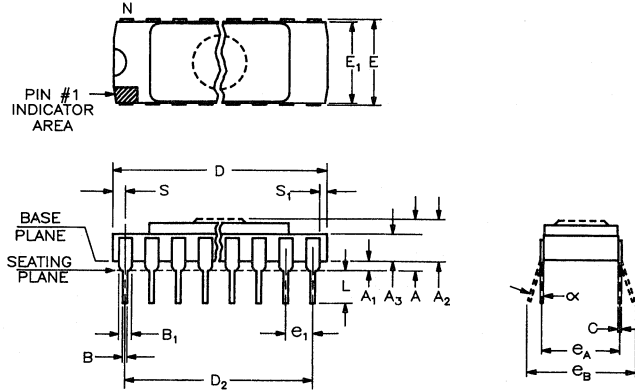


231369-2

2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.18	4.44	Solid Lid	0.125	0.175	Solid Lid
A	3.81	5.33	EPROM Lid	0.150	0.210	EPROM Lid
A ₁	1.02	1.52		0.040	0.060	
A ₂	2.16	2.92	Solid Lid	0.085	0.115	Solid Lid
A ₂	2.79	3.81	EPROM Lid	0.110	0.150	EPROM Lid
A ₃	1.91	2.54		0.075	0.100	
B	0.38	0.56		0.015	0.022	
B ₁	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	30.10	30.86		1.185	1.215	
D ₂	27.94		Reference	1.100		Reference
E	15.24	15.75		0.600	0.620	
E ₁	14.86	15.37		0.585	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	17.15		0.600	0.665	
L	3.18	4.06		0.125	0.160	
N	24			24		
S	0.76	1.78		0.030	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

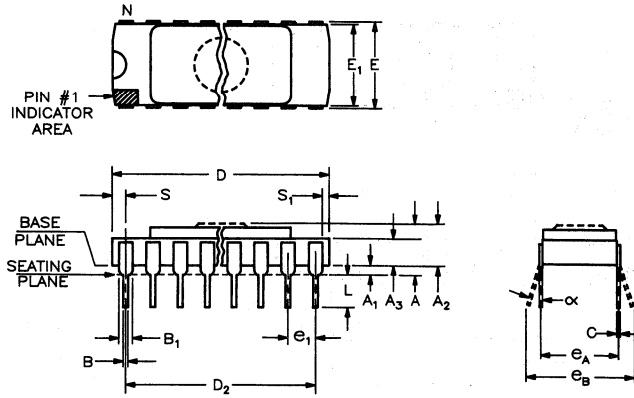
28 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.30	4.44	Solid Lid	0.130	0.175	Solid Lid
A	3.94	5.33	EPROM Lid	0.155	0.210	EPROM Lid
A ₁	1.02	1.52		0.040	0.060	
A ₂	2.29	2.92	Solid Lid	0.090	0.115	Solid Lid
A ₂	2.92	3.81	EPROM Lid	0.115	0.150	EPROM Lid
A ₃	2.03	2.54		0.080	0.100	
B	0.38	0.56		0.015	0.022	
B ₁	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	35.18	35.94		1.385	1.415	
D ₂	33.02		Reference	1.300		Reference
E	15.24	15.75		0.600	0.620	
E ₁	14.86	15.37		0.585	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	17.15		0.600	0.675	
L	3.18	4.06		0.125	0.160	
N	28			28		
S	0.76	1.78		0.030	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

32 LEAD CERAMIC DUAL IN-LINE PACKAGE

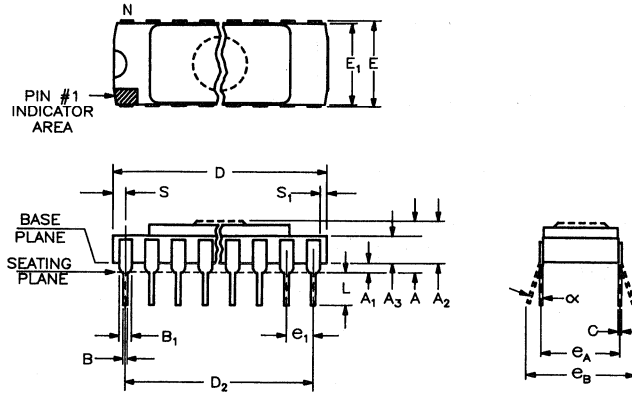


231369-2

2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.94	5.23	EPROM Lid	0.155	0.206	EPROM Lid
A ₁	1.02	1.52		0.040	0.060	
A ₂	3.00	3.71	EPROM Lid	0.118	0.146	EPROM Lid
A ₃	2.03	2.54		0.080	0.100	
B	0.38	0.56		0.015	0.022	
B ₁	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	40.28	41.00		1.586	1.614	
D ₂	38.10		Reference	1.500		Reference
E	15.24	15.75		0.600	0.620	
E ₁	14.86	15.37		0.585	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	17.15		0.600	0.675	
L	3.18	4.06		0.125	0.160	
N	32			32		
S	0.76	1.78		0.030	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

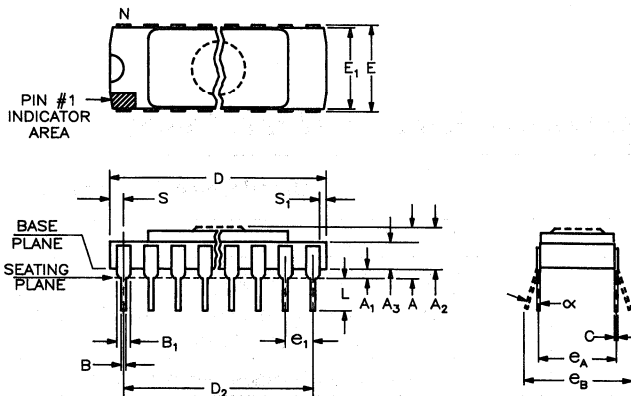
40 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.30	5.51	Solid Lid	0.130	0.217	Solid Lid
A	4.04	6.58	EPROM Lid	0.159	0.259	EPROM Lid
A ₁	1.02	1.52		0.040	0.060	
A ₂	2.29	3.99	Solid Lid	0.090	0.157	Solid Lid
A ₂	3.02	4.87	EPROM Lid	0.119	0.190	EPROM Lid
A ₃	2.03	3.66		0.080	0.144	
B	0.38	0.56		0.015	0.022	
B ₁	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	50.29	51.31		1.980	2.020	
D ₂	48.26		Reference	1.900		Reference
E	15.24	15.75		0.600	0.620	
E ₁	14.86	15.37		0.585	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	17.15		0.600	0.675	
L	3.18	4.06		0.125	0.160	
N	40			40		
S	0.76	1.78		0.030	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

48 LEAD CERAMIC DUAL IN-LINE PACKAGE



231369-2

2

Family: Ceramic Side Braze Dual In-Line						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.24	5.51	Solid Lid	0.167	0.217	Solid Lid
A	4.95	6.32	EPROM Lid	0.195	0.249	EPROM Lid
A ₁	1.02	1.52		0.040	0.060	
A ₂	3.23	3.99	Solid Lid	0.127	0.157	Solid Lid
A ₂	3.94	4.80	EPROM Lid	0.155	0.189	EPROM Lid
A ₃	2.95	3.66		0.116	0.144	
B	0.38	0.56		0.015	0.022	
B ₁	1.27		Typical	0.050		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	60.45	61.47		2.380	2.420	
D ₂	58.42		Reference	2.3		Reference
E	15.24	15.75		0.600	0.620	
E ₁	14.86	15.37		0.585	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	16.89		0.600	0.665	
L	3.18	4.06		0.125	0.160	
N	48			48		
S	0.76	1.78		0.030	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					



CERAMIC LAND GRID ARRAY PACKAGE (LGA)

Symbol List for Ceramic Land Grid Array Family

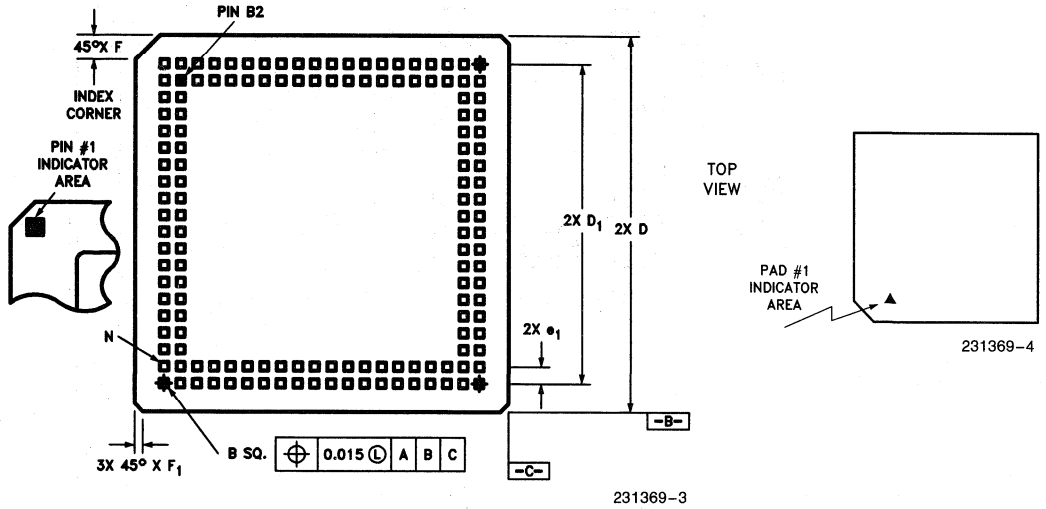
Letter or Symbol	Description of Dimensions
A	Overall Height
A ₁	Shoulder to Board Height
B ₁	Width of Terminal Lead Shoulder which Locate Seating Plane (Standoff Geometry Optional)
D	Largest Overall Package Dimension of Length
D ₁	Plastic Body Dimension
D ₂	Foot Print
e ₁	Linear Spacing between Centerline of Body Terminal Leads (Standoffs)
e _A	Linear Spacing of True Minimum Lead Position Center Line to Center Line
e _B	Linear Spacing between True Lead Position Outside of Lead to Outside of Lead
F	Index Corner
F ₁	Corner Chamfer Dimension
N	Total Number of Leads

Packaging Family Attributes	
Category	Land Grid Array
Acronym	LGA
Lead Configuration	N/A
Lead Counts	144, 168, 277
Land Finish	Gold Plate
Land Pitch	See Notes
Board Assembly	Custom Socket
Standard Registration	TBD

NOTES:

1. Multilayered Co-Fired Ceramic Body.
2. Land Pitch 0.050" - 144, 277
 0.100" - 168

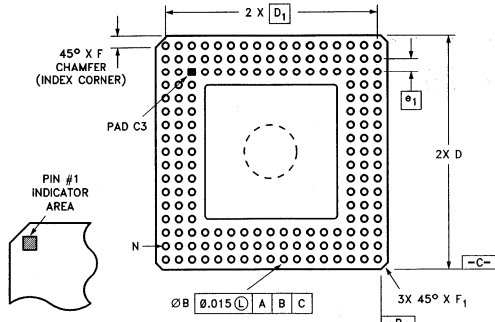
144 LEAD CERAMIC LAND GRID ARRAY (LGA) VIEW: CAVITY UP



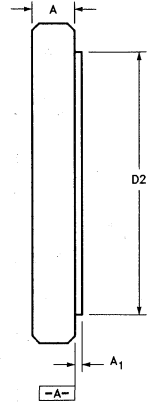
2

Family: Ceramic Land Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.46	3.58		0.097	0.125	
A ₁	0.23	0.43		0.009	0.017	
B	0.69	0.84		0.027	0.033	
D	28.96	29.46		1.140	1.160	
D ₁	24.13		BASIC	0.950		BASIC
D ₂		24.13			0.950	
e ₁	1.27		BASIC	0.050		BASIC
F	1.65	2.16		0.065	0.085	
F ₁	0.0025	0.076		0.010	0.030	
N	144			144		
ISSUE	IWS 7/25/90					

168 LEAD CERAMIC LAND GRID ARRAY (LGA) VIEW: CAVITY DOWN



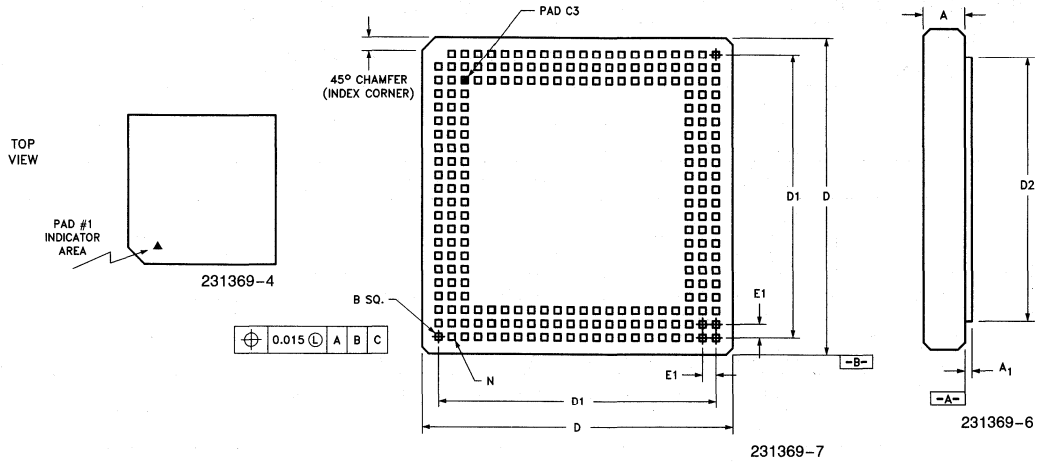
231369-5



231369-6

Family: Ceramic Land Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.79	3.56		0.110	0.140	
A ₁	0.23	0.43		0.009	0.017	
B	1.65	1.91		0.065	0.075	
D	44.20	44.83		1.740	1.765	
D ₁	40.64		BASIC	1.600		BASIC
D ₂		26.92			1.060	
e ₁	2.54		BASIC	0.100		BASIC
F	1.65	2.16		0.065	0.085	
F ₁	0.25	0.76		0.010	0.030	
N	168			168		
ISSUE	9/90					

**227 LEAD CERAMIC LAND GRID ARRAY (LGA)
VIEW: CAVITY UP**



2

Family: Ceramic Land Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.46	3.18		0.097	0.125	
A ₁	0.23	0.43		0.009	0.017	
B	0.69	0.84		0.027	0.033	
D	28.96	29.46		1.140	1.160	
D ₁	26.67		BASIC	1.050		BASIC
D ₂		24.13			0.950	
e ₁	1.27		BASIC	0.050		BASIC
F	1.65	2.16		0.065	0.085	
F ₁	0.25	0.76		0.010	0.30	
N	227			227		
ISSUE	IWS 9/90					



CERAMIC LEADLESS CHIP CARRIER

Symbol List for Ceramic Leadless Chip Carrier Family

Letter or Symbol	Description of Dimensions
A	Thickness of base body
A ₁	Total package height
A ₂	Distance from base body to highest point of body (lid)
B	Width of terminal lead pin
D	Largest overall package dimension of length
D ₁ , E ₁	A body length dimension, corner cutout to corner cutout or end lead center to end lead center
D ₂ , E ₂	A body length dimension, end lead center to end lead center
D ₃ , E ₃	A body length dimension, corner cutout to index corner cutout
D ₄ , E ₄	Ceramic body fixture
E	Largest overall package dimension of width
e	Linear spacing
e ₁	Linear spacing between edges of true lead positions (of corner terminal lead pads) lead corner to lead corner
h	Depth of major index feature
j	Width of minor index feature
L	Distance from package edge to end of effective pad
N	The total number of potentially useable lead positions
R ₁	Inner notch radius

NOTES:

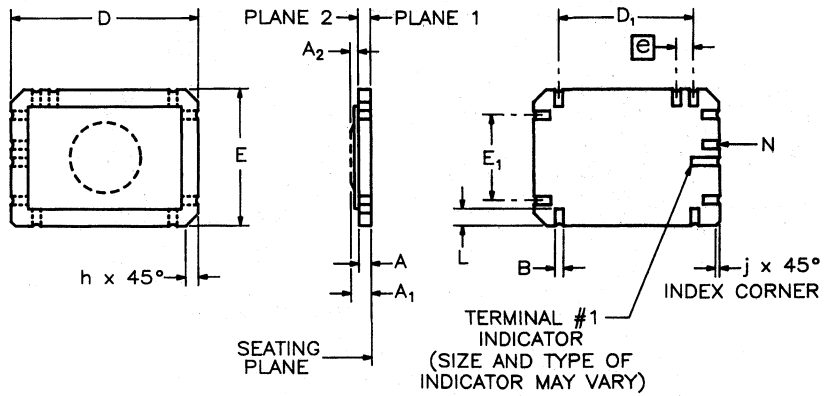
1. Controlling dimension: millimeter.
2. Dimension "e₁" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.430 inch.
4. Dimensions "B", "B₁" and "C" are nominal.
5. Corner configuration optional.

Packaging Family Attributes	
Category	Ceramic Leadless Chip Carrier
Acronym	LCC
Lead Configuration	N/A
Lead Counts	18, 20, 28, 32, 44, 68
Lead Finish	Gold Plate
Lead Pitch	0.050"
Board Assembly Type	Socket and Surface Mount
Standard Registration	—

NOTES:

1. 68L not certified for Surface Mount, must be socketed.
2. Multilayer Co-Fired Ceramic Body.

18 CERAMIC LEADLESS CHIP CARRIER

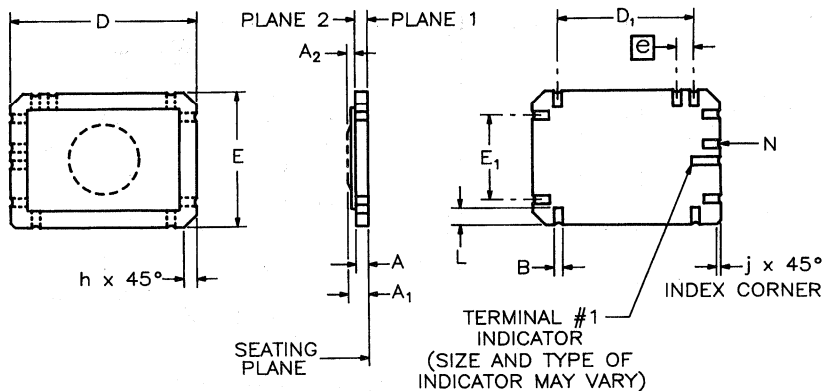


231369-8

2

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.35	1.78		0.053	0.070	
A ₁	1.60	1.88		0.063	0.074	
A ₂	0.25	0.36		0.010	0.014	
B	0.51	0.76		0.020	0.030	
D	10.54	11.18		0.415	0.440	
D ₁	5.08		Reference	0.200		Reference
E	6.99	7.62		0.275	0.300	
E ₁	3.81		Reference	0.150		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	18			18		
ISSUE	IWS 10/12/88					

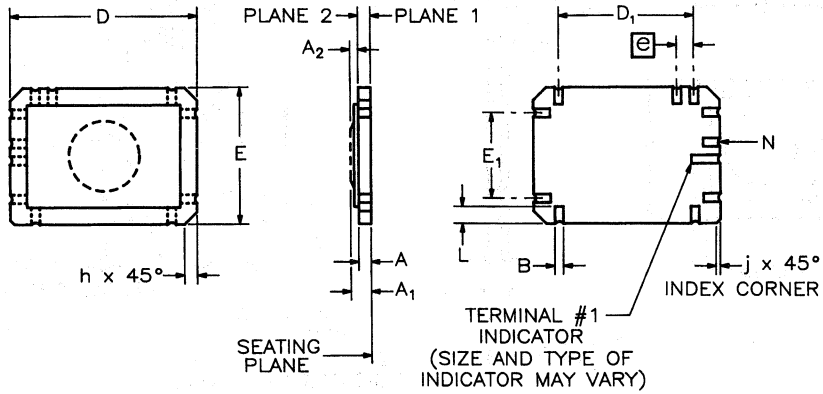
20 CERAMIC LEADLESS CHIP CARRIER



231369-8

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.35	1.78		0.053	0.070	
A ₁	1.60	1.88		0.063	0.074	
A ₂	0.25	0.36		0.010	0.014	
B	0.51	0.76		0.020	0.030	
D	10.54	11.18		0.415	0.440	
D ₁	6.35		Reference	0.250		Reference
E	7.11	7.62		0.280	0.300	
E ₁	3.81		Reference	0.150		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	20			20		
ISSUE	IWS 10/12/88					

32 CERAMIC LEADLESS CHIP CARRIER

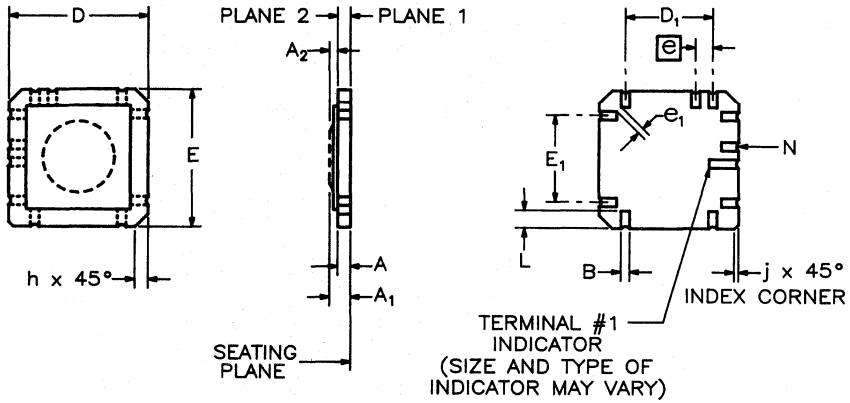


231369-8

2

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.45	2.03		0.057	0.080	
A ₁	1.70	2.39	Solid Lid	0.067	0.094	Solid Lid
A ₁	2.39	3.12	EPROM Lid	0.094	0.123	EPROM Lid
A ₂	0.25	0.36	Solid Lid	0.010	0.014	Solid Lid
A ₂	0.94	1.09	EPROM Lid	0.037	0.043	EPROM Lid
B	0.51	0.76		0.020	0.030	
D	13.72	14.22		0.540	0.560	
D ₁	10.16		Reference	0.400		Reference
E	11.18	11.68		0.440	0.460	
E ₁	7.62		Reference	0.300		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	32			32		
ISSUE	IWS 10/12/88					

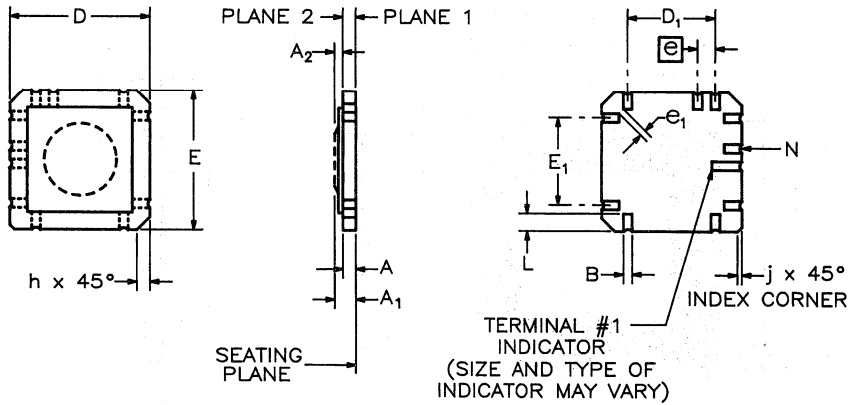
28 CERAMIC LEADLESS CHIP CARRIER



231369-9

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.35	1.78		0.053	0.070	
A ₁	1.60	2.13		0.063	0.084	
A ₂	0.25	0.36		0.010	0.014	
B	0.51	0.76		0.020	0.030	
D	11.18	11.68		0.440	0.460	
D ₁	7.62		Reference	0.300		Reference
E	11.18	11.68		0.440	0.460	
E ₁	7.62		Reference	0.300		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	28			28		
ISSUE	IWS 10/12/88					

44 CERAMIC LEADLESS CHIP CARRIER

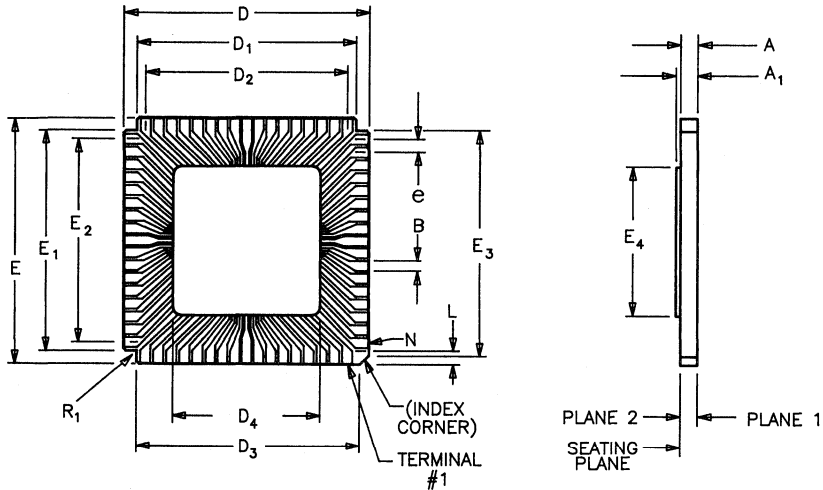


231369-9

2

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.52	2.54		0.060	0.100	
A ₁	1.78	2.90	Solid Lid	0.070	0.114	Solid Lid
A ₁	2.46	3.63	EPROM Lid	0.097	0.143	EPROM Lid
A ₂	0.25	0.36	Solid Lid	0.010	0.014	Solid Lid
A ₂	0.94	1.09	EPROM Lid	0.037	0.043	EPROM Lid
B	0.51	0.76		0.020	0.030	
D	16.13	16.89		0.635	0.665	
D ₁	12.70		Reference	0.500		Reference
E	16.13	16.89		0.635	0.665	
E ₁	12.70		Reference	0.500		Reference
[e]	1.09	1.45	Typical	0.043	0.057	Typical
L	1.02	2.29		0.040	0.090	
N	44			44		
ISSUE	IWS 10/12/88					

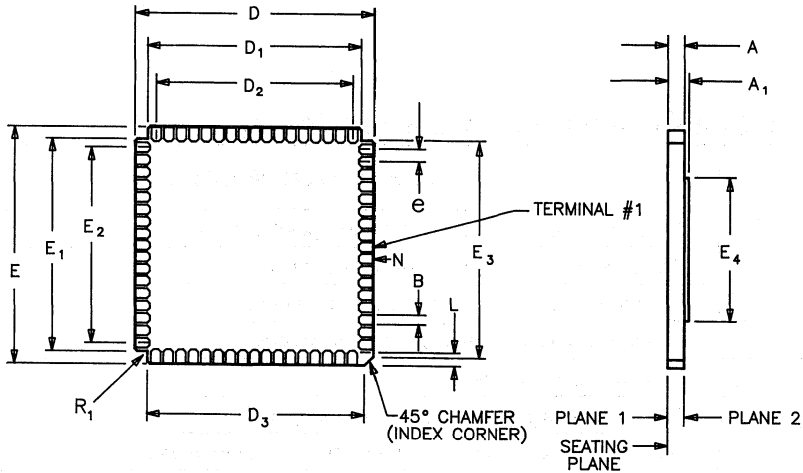
68 CERAMIC LEADLESS CHIP CARRIER



231369-10

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.37	1.68		0.054	0.066	
A ₁	2.16	2.72		0.085	0.107	
B	0.84	0.99	Typical	0.033	0.039	Typical
D	23.88	24.38		0.940	0.960	
D ₁	21.39	21.39		0.842	0.858	
D ₂	20.32		Reference	0.800		Reference
D ₃	21.92		Reference	0.863		Reference
D ₄	16.76	17.27		0.660	0.680	
E	23.88	24.38		0.940	0.960	
E ₁	21.39	21.79		0.842	0.858	
E ₂	20.32		Reference	0.800		Reference
E ₃	21.92		Reference	0.863		Reference
E ₄	16.76	17.27		0.660	0.680	
e	1.04	1.50	Typical	0.041	0.059	Typical
L	0.94			0.037		
N	68			68		
R ₁		0.25			0.010	
ISSUE	IWS 10/12/88					

68 CERAMIC LEADLESS CHIP CARRIER



231369-11

2

Family: Ceramic Leadless Chip Carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.91	2.41		0.075	0.095	
A ₁	2.92	3.68	W/EPROM	0.115	0.145	W/EPROM
B	0.84	1.12		0.033	0.044	
D	23.88	24.38		0.940	0.960	
D ₁	21.39	21.79		0.842	0.858	
D ₂	20.32		Reference	0.800		Reference
D ₃	22.05		Reference	0.868		Reference
E	23.88	24.38		0.940	0.960	
E ₁	21.39	21.79		0.842	0.858	
E ₂	20.32		Reference	0.800		Reference
E ₃	22.05		Reference	0.868		Reference
E ₄	14.33	15.14		0.564	0.596	
e	1.04	1.50	Typical	0.041	0.059	Typical
L	1.27			0.050		
N	68			68		
R ₁		0.25			0.010	
ISSUE	IWS 10/12/88					



CERAMIC PIN GRID ARRAY PACKAGE

Symbol List for Ceramic Pin Grid Array Family

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A ₁	Distance between seating plane and base plane
A ₂	Distance from base plane to highest point of body
A ₃	Distance from seating plane to bottom of body
B	Diameter of terminal lead pin
D	Largest overall package dimension of length
D ₁	A body length dimension, outer lead center to outer lead center
e ₁	Linear spacing between true lead position centerlines
L	Distance from seating plane to end of lead
S ₁	Other body dimension, outer lead center to edge of body

NOTES:

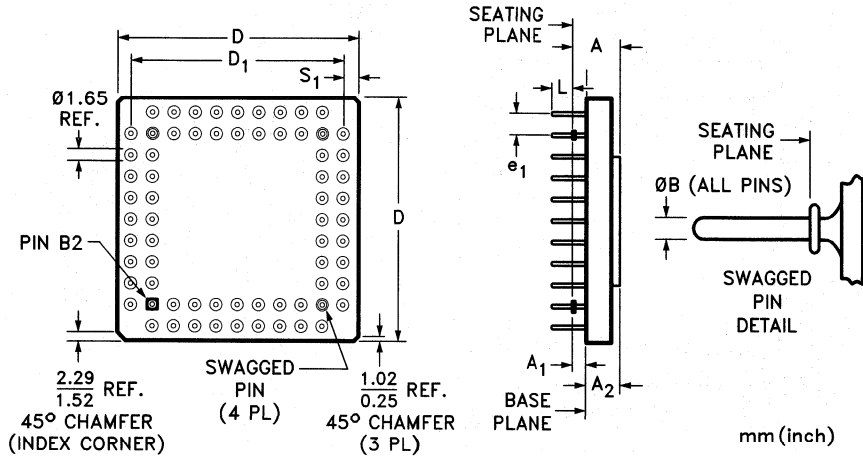
1. Controlling dimension: millimeter.
2. Dimension "e₁" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions "B", "B₁" and "C" are nominal.
5. Details of Pin 1 identifier are optional.

Packaging Family Attributes	
Category	Ceramic Pin Grid Array
Acronym	C-PGA or PGA
Lead Configuration	Array
Lead Counts	68, 88, 132, 168, 208, 240–280
Lead Finish	Gold Plate
Lead Pitch	0.100"
Board Assembly Type	Socket and Insertion Mount
Standard Registration	JEDEC and EIAJ

NOTES:

1. Alloy 42 or Kovar Leads.
2. Multilayer Co-Fired Ceramic Body.
3. 240–280 has variable pin count.

68 LEAD CERAMIC PIN GRID ARRAY PACKAGE

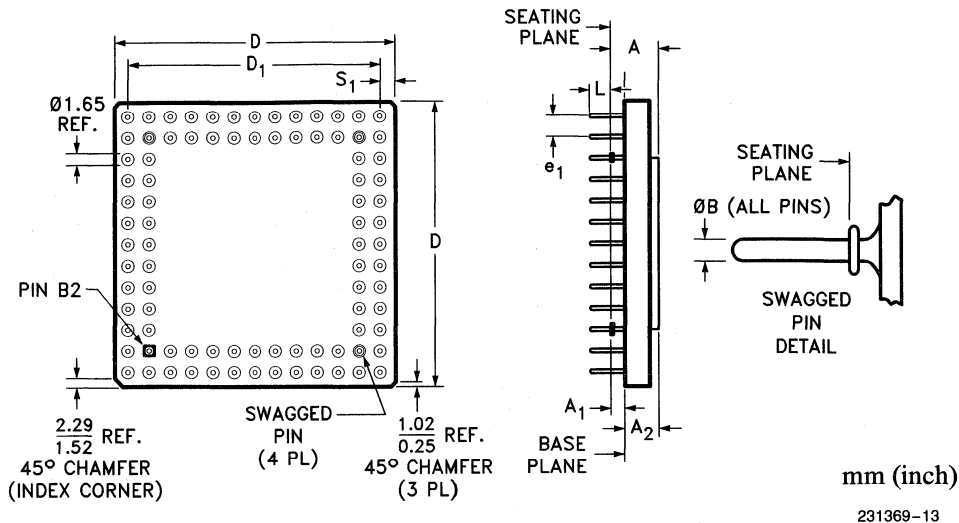


231369-12

2

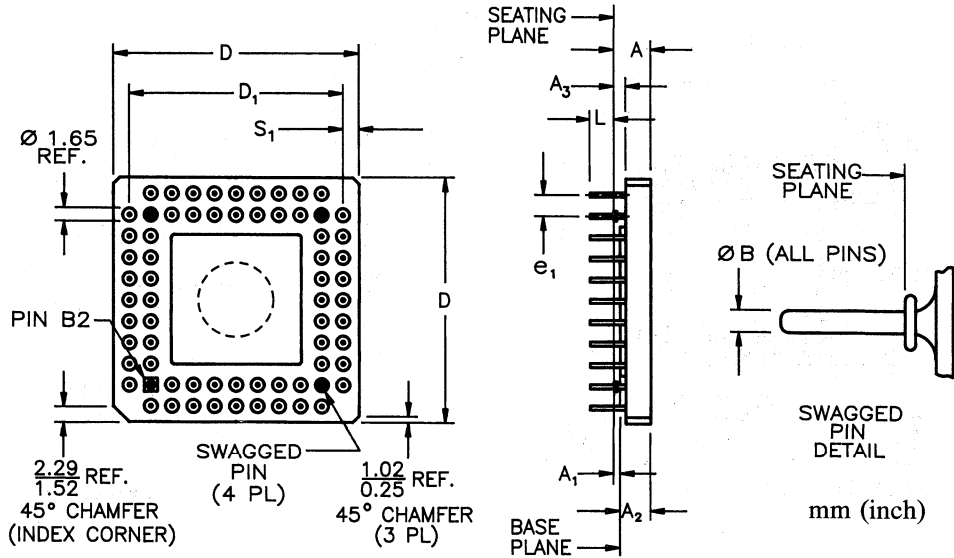
Family: Ceramic Pin Grid Array Package (Cavity Up)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	4.06	5.21	EPROM Lid	0.160	0.205	EPROM Lid
A	3.30	4.32	Solid Lid	0.130	0.170	Solid Lid
A ₁	1.14	1.40		0.045	0.055	
A ₂	2.16	3.18	Solid Lid	0.085	0.125	Solid Lid
A ₂	2.67	3.94	EPROM Lid	0.105	0.155	EPROM Lid
B	0.43	0.51		0.017	0.020	
D	28.96	29.59		1.140	1.165	
D ₁	25.27	25.53		0.995	1.005	
e ₁	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	68			68		
S ₁	1.27	2.54		0.050	0.100	
ISSUE	IWS	04/19/90				

88 LEAD CERAMIC PIN GRID ARRAY PACKAGE



Family: Ceramic Pin Grid Array Package (Cavity Up)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	4.06	5.21	EPROM Lid	0.160	0.205	EPROM Lid
A	3.30	4.32	Solid Lid	0.130	0.170	Solid Lid
A ₁	1.14	1.4		0.045	0.055	
A ₂	2.16	3.18	Solid Lid	0.085	0.125	Solid Lid
A ₂	2.67	3.94	EPROM Lid	0.105	0.155	EPROM Lid
B	0.43	0.51		0.017	0.020	
D	34.04	34.67		1.340	1.365	
D ₁	30.35	30.61		1.195	1.205	
e ₁	2.29	2.79		0.090	0.110	
L	3.05	3.56		0.120	0.140	
N	88			88		
S ₁	1.27	2.54		0.050	0.100	
ISSUE	IWS 10/21/88					

68 LEAD CERAMIC PIN GRID ARRAY PACKAGE

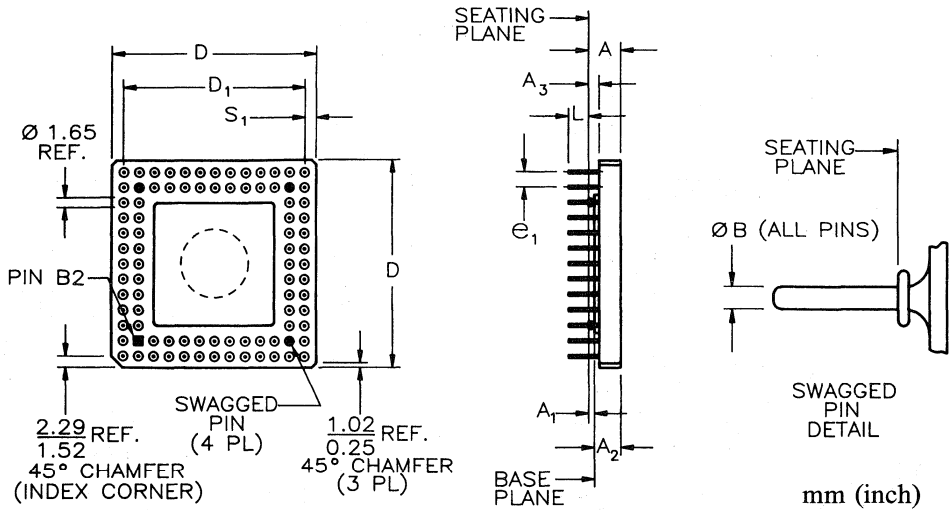


231369-14

2

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A ₁	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A ₁		0.41	EPROM Lid		0.016	EPROM Lid
A ₂	2.72	3.43	Solid Lid	0.107	0.135	Solid Lid
A ₂	3.43	4.32	EPROM Lid	0.135	0.170	EPROM Lid
A ₃	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	28.83	29.59		1.135	1.165	
D ₁	25.27	25.53		0.995	1.005	
e ₁	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	68			68		
S ₁	1.27	2.54		0.050	0.100	
ISSUE	IWS 12/08/88					

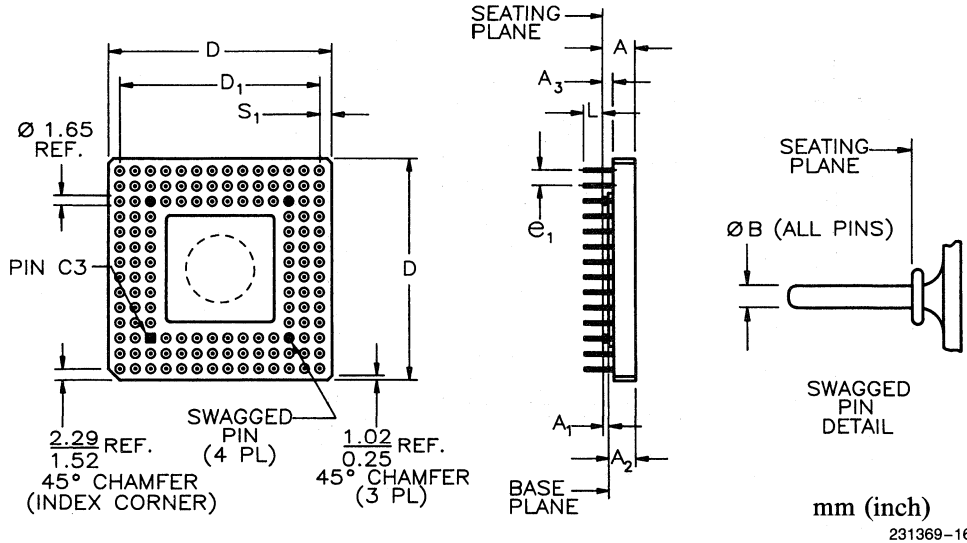
88 LEAD CERAMIC PIN GRID ARRAY PACKAGE



231369-15

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A ₁	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A ₂	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A ₃	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	33.91	34.67		1.335	1.365	
D ₁	30.35	30.61		1.195	1.205	
e ₁	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	88			88		
S ₁	1.27	2.54		0.050	0.100	
ISSUE	IWS 10/12/88					

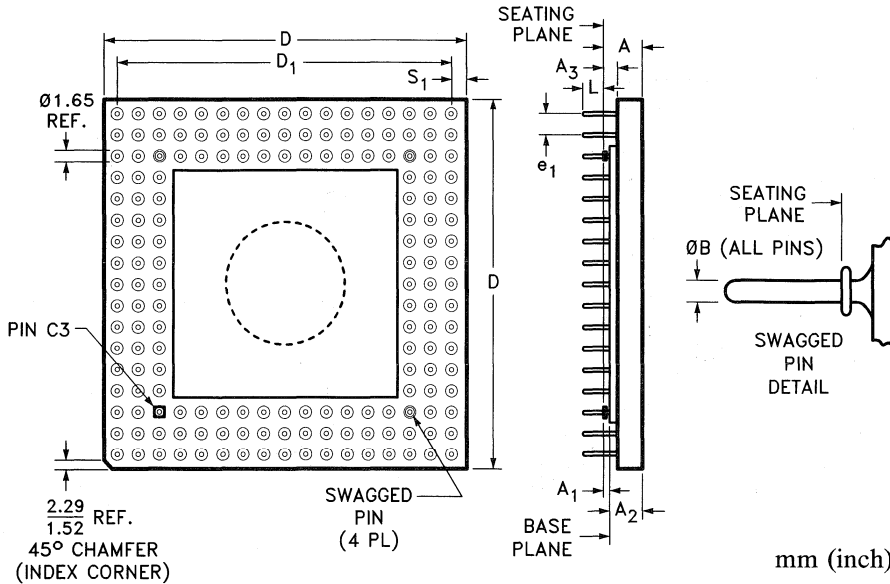
132 LEAD CERAMIC PIN GRID ARRAY PACKAGE



2

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A ₁	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A ₂	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A ₃	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	36.45	37.21		1.435	1.465	
D ₁	32.89	33.15		1.295	1.305	
e ₁	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	132			132		
S ₁	1.27	2.54		0.050	0.100	
ISSUE	IWS 10/12/88					

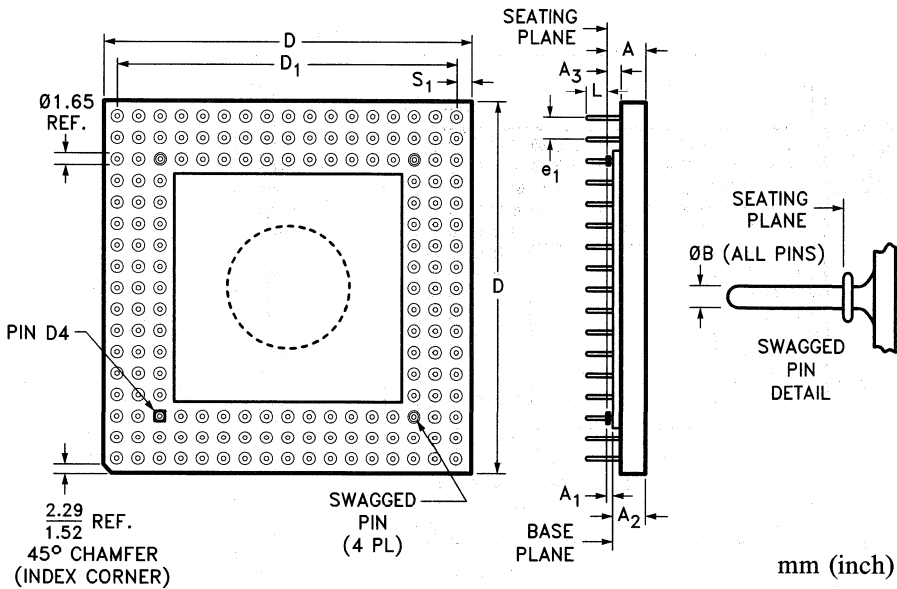
168 LEAD CERAMIC PIN GRID ARRAY PACKAGE



231369-17

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A ₁	0.64	1.14	Solid Lid	0.025	0.045	Solid Lid
A ₂	0.23	0.30	Solid Lid	0.110	0.140	Solid Lid
A ₃	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.07	44.83		1.735	1.765	
D ₁	40.51	40.77		1.595	1.605	
e ₁	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	168			168		
S ₁	1.52	2.54		0.060	0.100	
ISSUE	IWS 11/29/88					

208 LEAD CERAMIC PIN GRID ARRAY PACKAGE

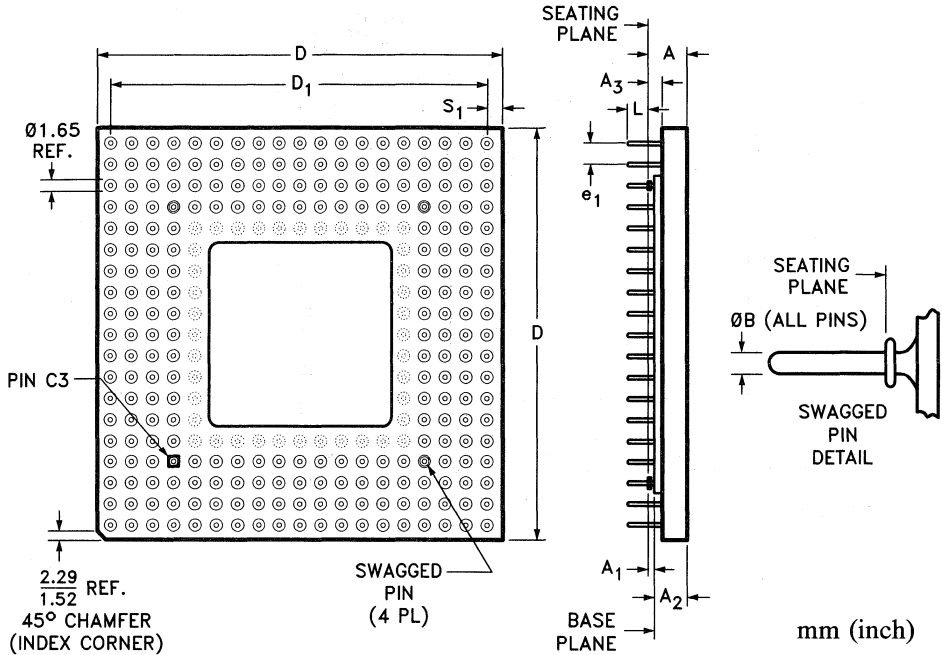


231369-18

2

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A ₁	0.64	1.14	Solid Lid	0.025	0.045	Solid Lid
A ₂	0.23	0.30	Solid Lid	0.110	0.140	Solid Lid
A ₃	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.07	44.83		1.735	1.765	
D ₁	40.51	40.77		1.595	1.605	
e ₁	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	208			208		
S ₁	1.52	2.54		0.060	0.100	
ISSUE	IWS 8/1/90					

1.95" SQ CERAMIC PIN GRID ARRAY PACKAGE



231369-19

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A ₁	0.64	1.14	Solid Lid	0.025	0.045	Solid Lid
A ₂	0.23	0.30	Solid Lid	0.110	0.140	Solid Lid
A ₃	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	49.53	50.17		1.950	1.975	
D ₁	45.59	45.85		1.795	1.805	
e ₁	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	240	280		240	280	
S ₁	1.52	2.54		0.060	0.100	
ISSUE	IWS 9/90					



CERAMIC PIN GRID ARRAY MODULE

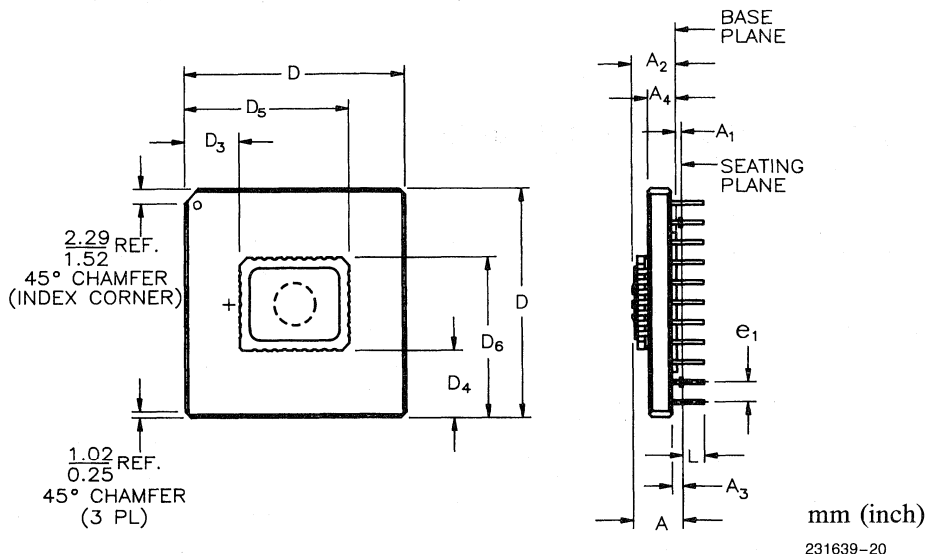
Symbol List for Pin Grid Array Module

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A ₁	Distance between seating plane and base plane
A ₂	Distance from base plane to highest point of body
A ₃	PGA body thickness including lid
A ₄	Distance from seating plane to base of body
D	Largest overall package dimension of length
D ₃	PGA to LCC start (LCC long dim)
D ₄	PGA to LCC start (LCC short dim)
D ₅	PGA to LCC end (LCC long dim)
D ₆	PGA to LCC end (LCC short dim)
e ₁	Linear spacing between centerlines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead

NOTES:

1. Controlling dimension: millimeter.
2. Dimension "e₁" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions "B", "B₁" and "C" are nominal.

CERAMIC PIN GRID ARRAY MODULE



mm (inch)
231639-20

Family: Ceramic Pin Grid Array Module						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	6.10	7.62		0.240	0.300	
A ₁	0.64	1.19		0.025	0.047	
A ₂	5.21	6.60		0.205	0.260	
A ₃	1.14	1.40		0.045	0.055	
A ₄	2.72	3.56		0.107	0.140	
D	28.83	29.59		1.135	1.165	
D ₃	6.35	8.64		0.250	0.340	
D ₄	7.37	9.40		0.290	0.370	
D ₅	20.07	23.62		0.790	0.930	
D ₆	18.54	22.61		0.730	0.890	
e ₁	2.29	2.79		0.090	0.110	
L	2.41	3.18		0.095	0.125	
N	68 PGA			68 PGA		
N	32 LCC			32 LCC		
ISSUE	10/12/88					



CERAMIC QUADPACK PACKAGE

Symbol List for Ceramic Quadpack Family

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package dimension of length
D ₁	Largest overall package dimension of length excluding leads
D ₂	A body length dimension, outer lead center to outer lead center
e ₁	Linear spacing between centerlines of terminal leads
L	Lead dimension free lead length
S	Distance from true position centerline of end lead position to the extremity of the body
S ₁	Linear spacing of true maximum lead position from lead edge to package edge

2

NOTES:

Controlling dimension: millimeter.
Dimension "e₁" ("e") is non-cumulative.
Pin numbering is ascending in the counterclockwise direction.
Dimensions "B", "B₁" and "C" are nominal.

Packaging Family Attributes	
Category	Ceramic Quadpack
Acronym	CQFP
Lead Configuration	Quad
Lead Counts	68
Lead Finish	Gold Plate or SolderCoat
Lead Pitch	0.050"
Board Assembly Type	Socket and Surface Mount
Standard Registration	JEDEC

NOTES:

1. Alloy 42 or Kovar Leads.
2. Sold unformed in carrier.

68 LEAD CERAMIC QUADPACK PACKAGE

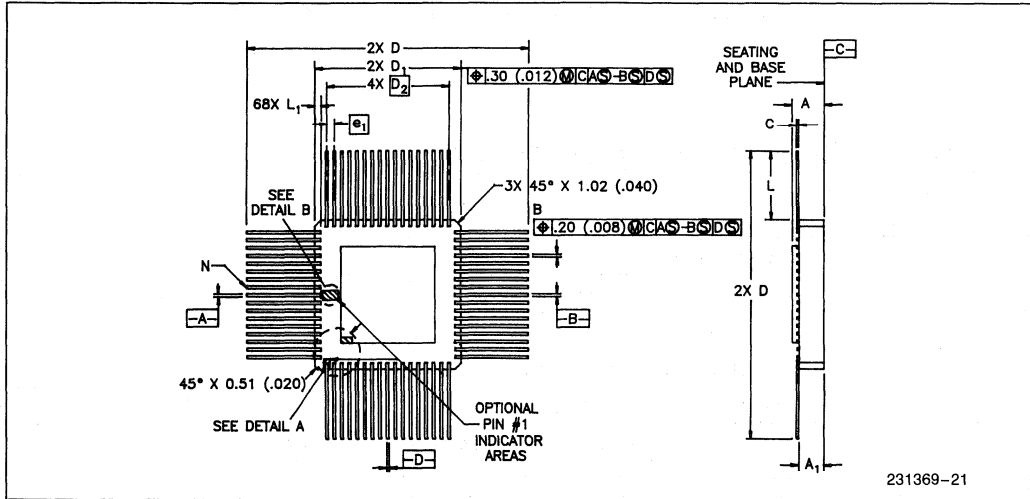


Figure 1. Principle Dimensions and Datums

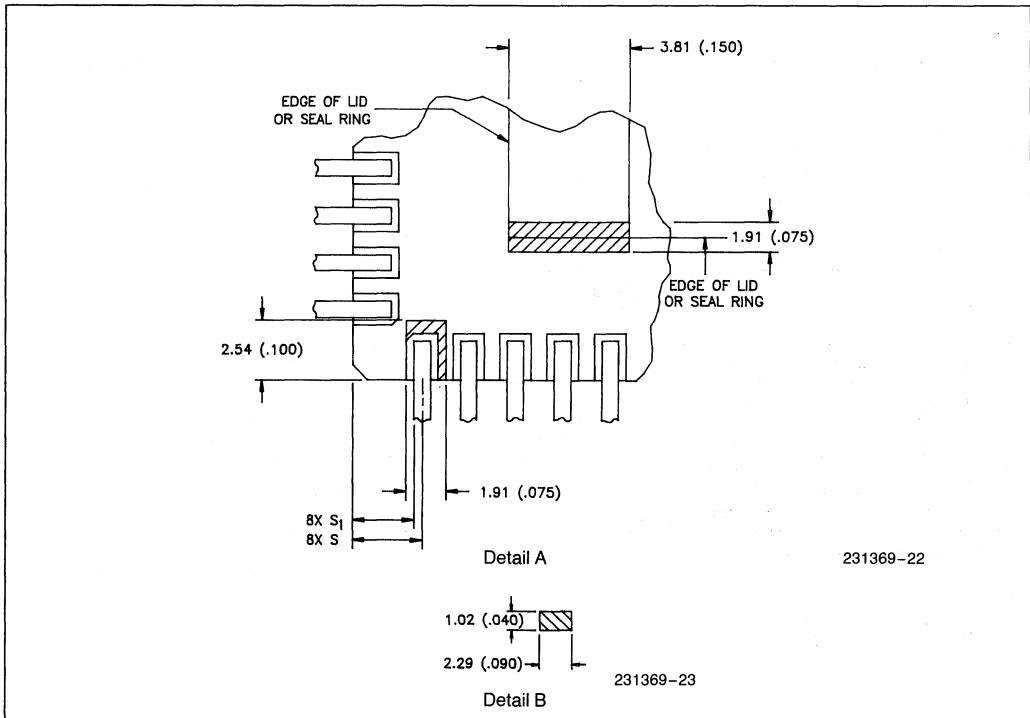


Figure 2. Details A, B

CERAMIC QUADPACK PACKAGE

Family: 68 Lead Ceramic Quadpack Family						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.03	2.69	Solid Lid	0.080	0.106	Solid Lid
A	2.29	3.68	EPROM Lid	0.090	0.145	EPROM Lid
A ₁	1.78	2.29		0.070	0.090	
B	0.41	0.53	68 Places	0.016	0.021	68 Places
B ₁	1.02	1.52	Typical	0.040	0.060	Typical
B ₂	0.76	1.02	Typical	0.030	0.040	Typical
B ₃	0.13	0.51	Typical	0.005	0.020	Typical
C	0.20	0.31		0.008	0.012	
D	41.66	47.50		1.640	1.870	
D ₁	23.52	24.64		0.926	0.970	
D ₂	20.32		BSC	0.800		BSC
e ₁	1.27 BSC		64 Places	0.050 BSC		64 Places
L	8.89	11.43		0.350	0.450	
L ₁	1.02	1.52		0.040	0.060	
N	68			68		
S	1.91		REF	0.075		REF
S ₁	1.27			0.050		
ISSUE	IWS 10/12/88					

2



CERAMIC QUAD FLATPACK PACKAGE

Symbol List for Quadpack Family (Military)

Letter or Symbol	Description of Dimensions
A	Distance from Seating Plane to Highest Point of Body (Lid)
A ₁	Ceramic Body Thickness
A ₂	Distance from Top of Ceramic to Bottom of Lead
B	Width of Terminal Leads
C	Thickness of Terminal Leads
D	Largest Overall Package Dimension of Length
D ₁	Largest Overall Package Dimension of Length Excluding Leads
D ₂	A Body Length Dimension, Outer Lead Center to Outer Lead Center
e ₁	Linear Spacing between Centerlines of Terminal Leads
H	Distance from Body Centerline to Locator Holes
H ₁	Distance between Opposite Locator Holes
H ₂	Distance from End Lead Centerline to Locator Holes
L	Lead Dimension Free Lead Length
S	Distance from True Position Centerline of End Lead Position to the Extremity of the Body
S ₁	Linear Spacing of True Maximum Lead Position from Lead Edge to Package Edge

NOTES:

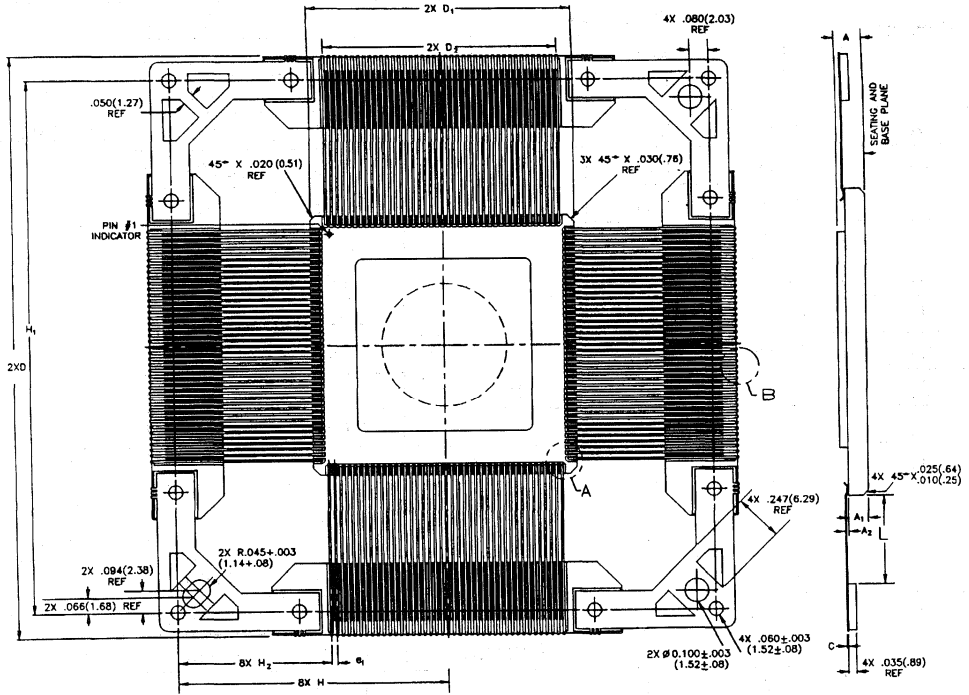
1. Dimension "e₁" ("e") is non-cumulative.
2. Pin numbering is ascending in the counterclockwise direction.

Packaging Family Attributes	
Category	Ceramic Quad Flatpack (Military)
Acronym	CQFP
Lead Configuration	Quad
Lead Counts	164, 196
Lead Finish	SolderCoat or SolderPlate
Lead Pitch	0.025"
Board Assembly Type	Socket and Surface Mount
Standard Registration	JEDEC

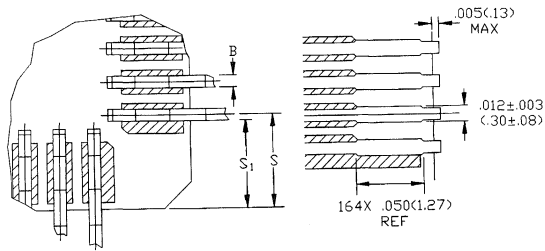
NOTES:

1. Kovar Leads.
2. Multilayer Co-Fired Alumina Ceramic Body.
3. 164L—SolderCoat or SolderPlate (unformed only in carrier).
4. 196L—SolderPlate only (formed and unformed).
5. Military use only.

**164 LEAD CERAMIC QUADPACK PACKAGE
VERSION: CAVITY UP, WITH N/C TIE BAR**



231369-24



DETAIL A

DETAIL B

231369-25

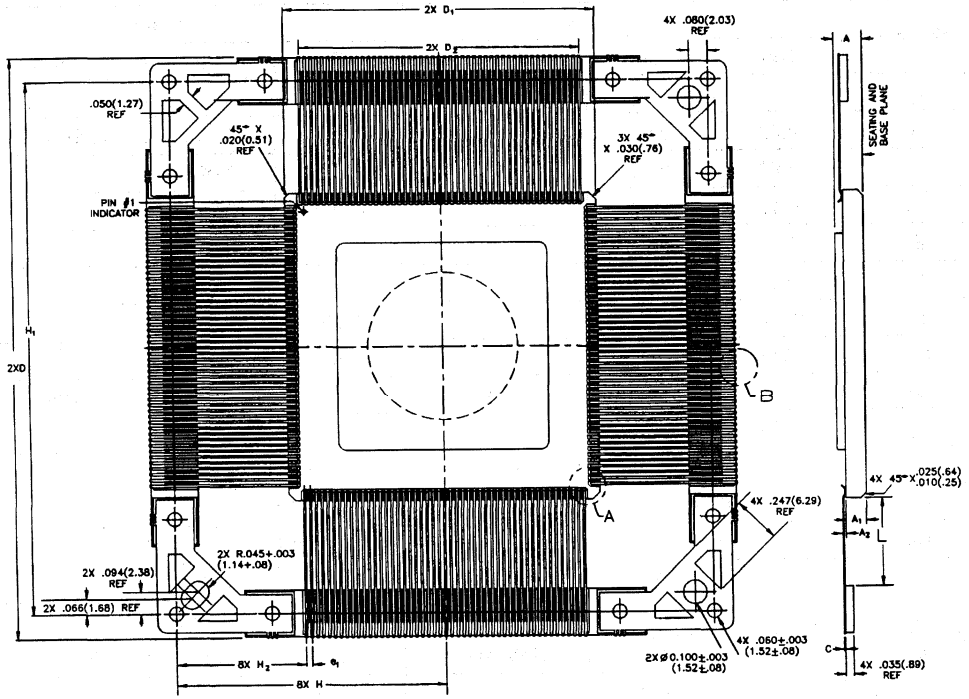
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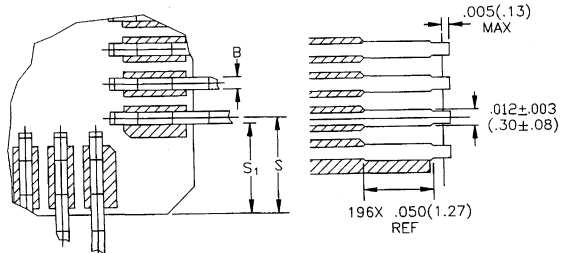
164 LEAD CERAMIC QUADPACK PACKAGE
VERSION: CAVITY UP, WITH N/C TIE BAR (Continued)

Family: Ceramic Quadpack (Military)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.92	Solid Lid	0.088	0.115	Solid Lid
A	2.92	3.56	EPROM Lid	0.115	0.140	EPROM Lid
A ₁	1.98	2.39		0.078	0.094	
A ₂	0.15	0.30		0.006	0.012	
B	0.18	0.25		0.007	0.010	
C	0.10	0.15		0.004	0.006	
D	63.50	64.01		2.500	2.520	
D ₁	28.45	28.96		1.120	1.140	
D ₂	25.40		Basic	1.000		Basic
e ₁	0.58	0.69		0.023	0.027	
H	29.21		Basic	1.150		Basic
H ₁	58.42		Basic	2.30		Basic
H ₂	16.51		Basic	0.650		Basic
L	9.27	10.03		0.365	0.395	
N	164			164		
S	1.52	2.03	Reference	0.060	0.080	Reference
S ₁	1.52	1.93		0.060	0.076	
ISSUE	IWS 7/90					

**196 LEAD CERAMIC QUADPACK PACKAGE
VERSION: CAVITY UP, WITH N/C TIE BAR**



231369-26



DETAIL A

DETAIL B

231369-27

2



196 LEAD CERAMIC QUADPACK PACKAGE
VERSION: CAVITY UP, WITH N/C TIE BAR (Continued)

Family: Ceramic Quadpack (Military)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.92	Solid Lid	0.088	0.115	Solid Lid
A	2.92	3.56	EPROM Lid	0.115	0.140	EPROM Lid
A ₁	1.96	2.39		0.077	0.094	
A ₂	0.15	0.30		0.006	0.012	
B	0.20	0.25		0.008	0.010	
C	0.10	0.20		0.004	0.008	
D	63.50	64.01		2.500	2.520	
D ₁	33.65	34.16		1.325	1.345	
D ₂	30.48		Basic	1.200		Basic
e ₁	0.58	0.69		0.023	0.027	
H	29.21		Basic	1.150		Basic
H ₁	58.42		Basic	2.30		Basic
H ₂	19.05		Basic	0.750		Basic
L	9.27	10.03		0.365	0.395	
N	196			196		
S	1.27	2.03	Reference	0.050	0.080	Reference
S ₁	1.14	1.93		0.045	0.076	
ISSUE	IWS 7/90					

NOTE:

1. Currently for Military application only.



CERDIP DUAL IN-LINE PACKAGE

Symbol List for Cerdip Dual In-Line Family

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
A ₁	Distance between seating plane and base plane
A ₂	Distance from base plane to highest point of body (lid)
A ₃	Base body thickness
B	Width of terminal leads
B ₁	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package dimension of length
D ₂	A body length dimension, end lead center to end lead center
E	Largest overall package width dimension outside of lead
E ₁	Body width dimensions not including leads
e _A	Linear spacing of true minimum lead position center line to center line
e _B	Linear spacing between true lead position outside of lead to outside of lead
e ₁	Linear spacing between centerlines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	The total number of potentially useable lead positions
S	Distance from true position centerline of No. 1 lead position to the extremity of the body
S ₁	Distance from other end lead edge positions to the extremity of the body
α	Angular spacing between minimum and maximum lead positions measured at the gauge plane

2

NOTES:

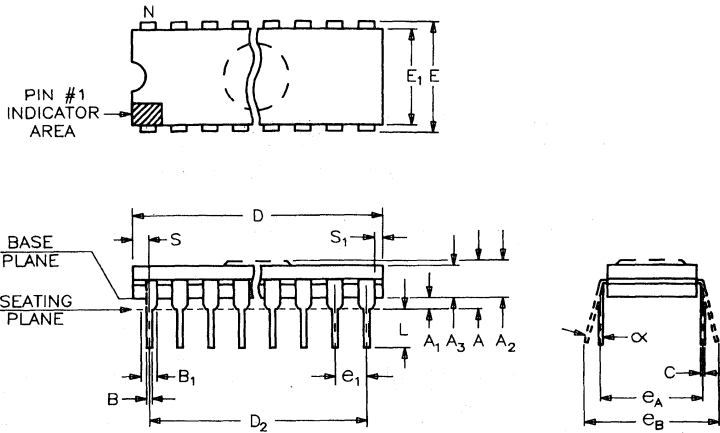
1. Controlling dimension: millimeter.
2. Dimension "e₁" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimension "B₁" is nominal.

Packaging Family Attributes	
Category	Cerdip
Acronym	Cerdip
Lead Configuration	Dual-In-Line
Lead Counts	16, 18, 20, 22, 24, 32, 40, 44
Lead Finish	Tin Plate of SolderPlate
Lead Pitch	0.100"
Board Assembly Type	Socket and Surface Mount
Standard Registration	JEDEC and EIAJ

NOTES:

1. Alloy 42 Leads.
2. Pressed Ceramic Body.
3. UV Window available for reprogramming.

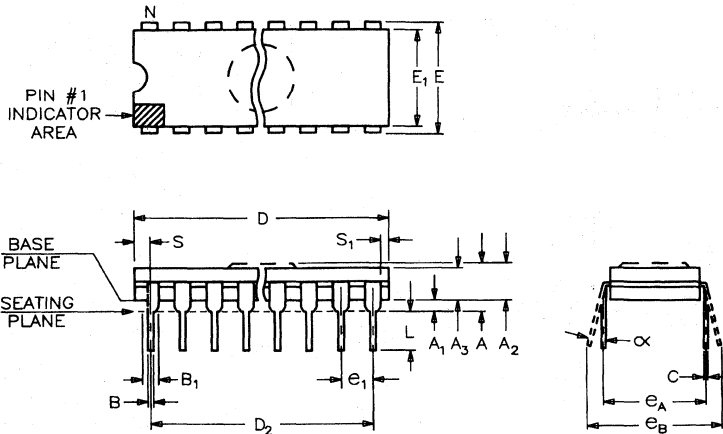
16 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-28

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.56	4.44		0.140	0.175	
A ₃	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	19.05	19.94		0.750	0.785	
D ₂	17.78		Reference	0.700		Reference
E	7.62	8.13		0.300	0.320	
E ₁	7.11	7.90		0.280	0.311	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.87		Reference	0.310		Reference
e _B	8.13	10.16		0.320	0.400	
L	3.18	3.81		0.125	0.150	
N	16		1/2 Leads	16		1/2 Leads
S	0.25	1.27		0.010	0.050	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

18 LEAD CERDIP DUAL IN-LINE PACKAGE

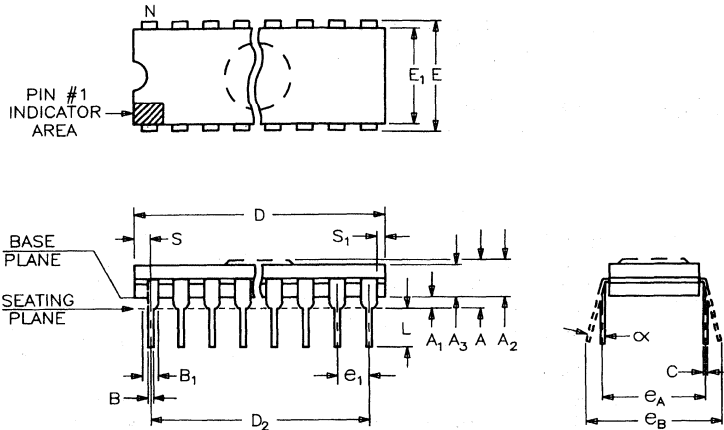


231369-28

2

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.56	4.44		0.140	0.175	
A ₃	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	22.35	23.24		0.880	0.915	
D ₂	20.32		Reference	0.800		Reference
E	7.62	8.13		0.300	0.320	
E ₁	7.11	7.90		0.280	0.311	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.87		Reference	0.310		Reference
e _B	8.13	10.16		0.320	0.400	
L	3.18	3.81		0.125	0.150	
N	18		½ Leads	18		½ Leads
S	0.64	1.78		0.025	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

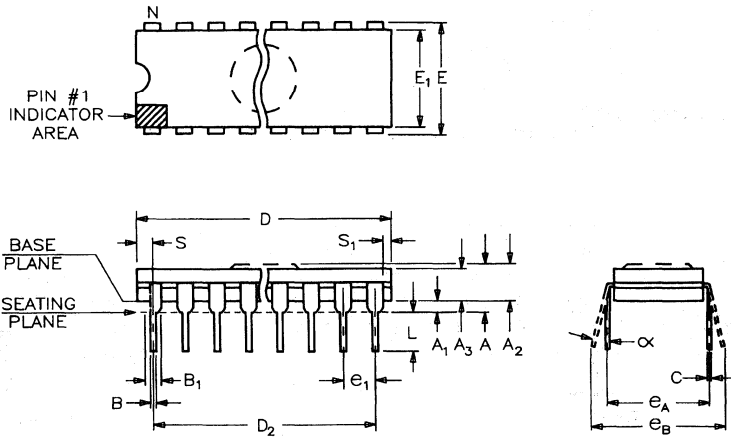
20 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-28

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.56	4.24		0.140	0.167	
A ₃	3.56	4.24		0.140	0.167	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	24.38	25.27		0.960	0.995	
D ₂	22.86		Reference	0.900		Reference
E	7.62	8.13		0.300	0.320	
E ₁	7.11	7.90		0.280	0.311	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.87		Reference	0.310		Reference
e _B	8.13	10.16		0.320	0.400	
L	3.18	3.81		0.125	0.150	
N	20		½ Leads	20		½ Leads
S	0.38	1.78		0.015	0.070	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

22 LEAD CERDIP DUAL IN-LINE PACKAGE

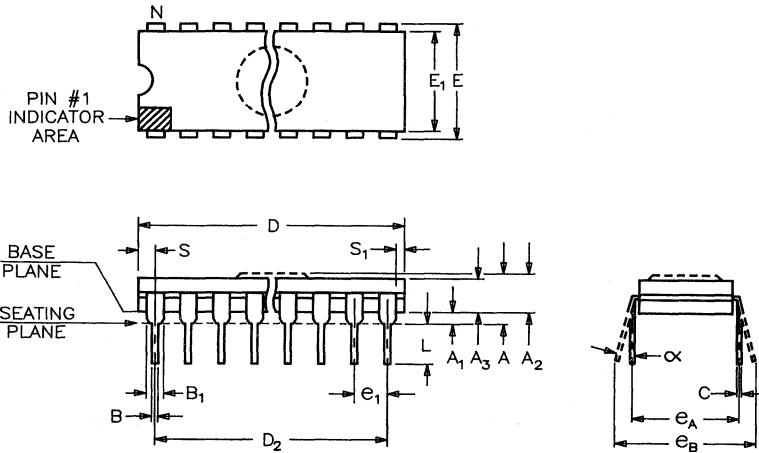


231369-28

2

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.81	4.57		0.150	0.180	
A ₃	3.81	4.57		0.150	0.180	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	26.92	27.81		1.060	1.095	
D ₂	25.40		Reference	1.000		Reference
E	10.16	10.67		0.400	0.420	
E ₁	9.53	10.29		0.375	0.405	
e ₁	2.29	2.79		0.090	0.110	
e _A	10.41		Reference	0.410		Reference
e _B	10.67	12.70		0.420	0.500	
L	3.18	3.81		0.125	0.150	
N	22		½ Leads/400 MIL	22		½ Leads/400 MIL
S	0.38	1.52		0.015	0.060	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

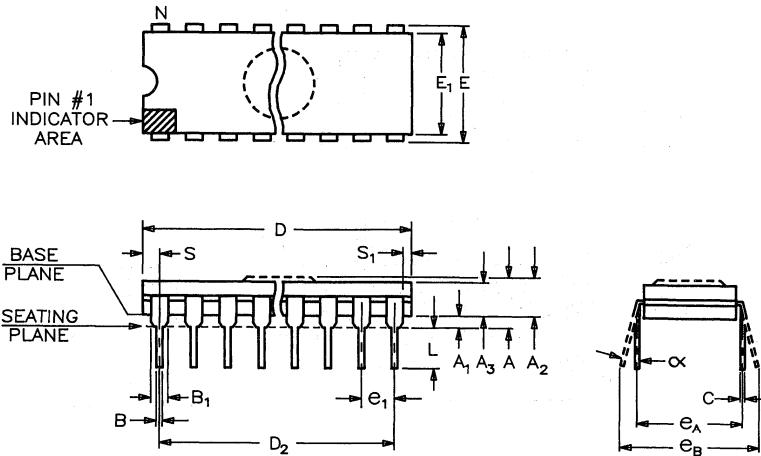
24 LEAD CERDIP DUAL IN-LINE PACKAGE (300 MIL)



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A ₁	0.38			0.015		
A ₂	3.56	4.83		0.140	0.190	
A ₃	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	Typical
B ₁	1.42		Typical	0.056		Typical
C	0.23	0.30	Typical	0.009	0.012	
D	31.50	32.64		1.240	1.285	
D ₂	27.94		Reference	1.100		Reference
E	7.62	8.13		0.300	0.320	
E ₁	7.11	7.87		0.280	0.310	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.87		Reference	0.310		Reference
e _B	8.13	10.16		0.320	0.400	
L	3.18	4.06		0.125	0.160	
N	24		300 MIL	24		300 MIL
S		2.29			0.090	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

24 LEAD CERDIP DUAL IN-LINE PACKAGE (600 MIL)

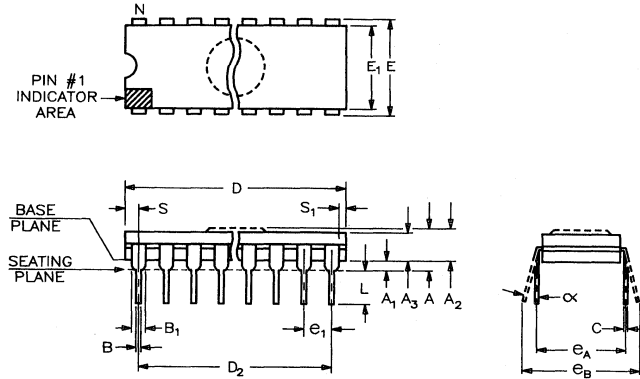


231369-29

2

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.56	4.70		0.140	0.185	
A ₃	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	31.50	32.64		1.240	1.285	
D ₂	27.94		Reference	1.100		Reference
E	15.24	15.75		0.600	0.620	
E ₁	13.08	15.24		0.515	0.600	
e ₁	2.29	2.79		0.090	0.110	
e _A	15.49		Reference	0.610		Reference
e _B	15.75	17.78		0.620	0.700	
L	3.18	3.81		0.125	0.150	
N	24		600 MIL	24		600 MIL
S	1.40	2.29		0.055	0.090	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

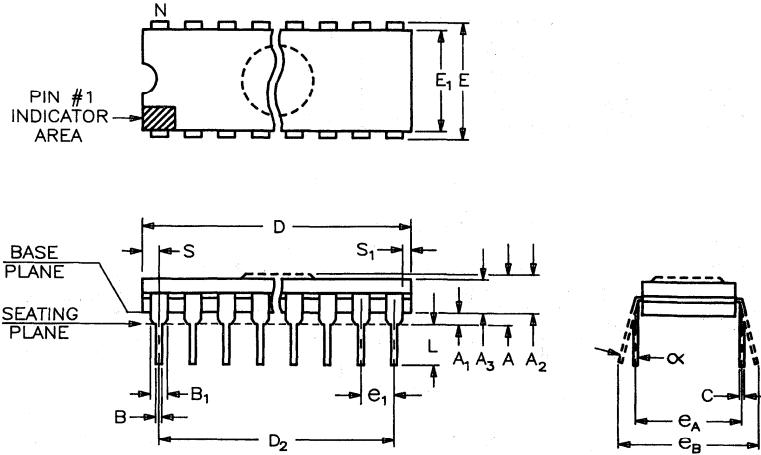
**28 LEAD CERDIP DUAL IN-LINE PACKAGE (300 MIL)
VERSION: SKINNY DIP**



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A ₁	0.38			0.015		
A ₂	3.56	4.83		0.140	0.190	
A ₃	3.56	4.44		0.140	0.175	
B	0.41	0.51		0.016	0.020	Typical
B ₁	1.42		Typical	0.056		Typical
C	0.23	0.30	Typical	0.009	0.012	
D	36.58	37.72		1.440	1.485	
D ₂	33.02		Reference	1.300		Reference
E	7.62	8.13		0.300	0.320	
E ₁	7.11	7.87		0.280	0.310	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.87		Reference	0.310		Reference
e _B	8.13	10.16		0.320	0.400	
L	3.18	4.06		0.125	0.160	
N	28		300 MIL	28		300 MIL
S		2.29			0.090	
S ₁	0.13			0.005		
ISSUE	IWS 9/19/90					

28 LEAD CERDIP DUAL IN-LINE PACKAGE (600 MIL)

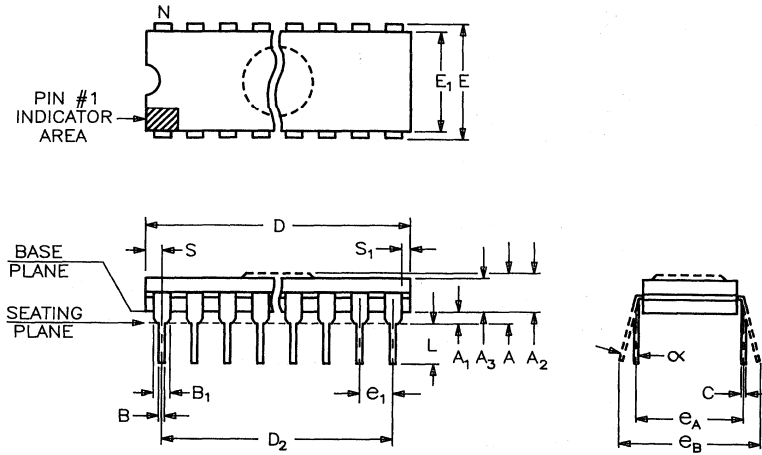


231369-29

2

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A ₁	0.38			0.015		
A ₂	3.56	4.95		0.140	0.195	
A ₃	3.56	4.70		0.140	0.185	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	36.58	37.72		1.440	1.485	
D ₂	33.02		Reference	1.300		Reference
E	15.24	15.75		0.600	0.620	
E ₁	13.08	15.37		0.515	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	15.49		Reference	0.610		Reference
e _B	15.75	17.78		0.620	0.700	
L	3.18	4.32		0.125	0.170	
N	28			28		
S	1.40	2.29		0.055	0.090	
S ₁	0.13			0.005		
ISSUE	IWS	04/19/90				

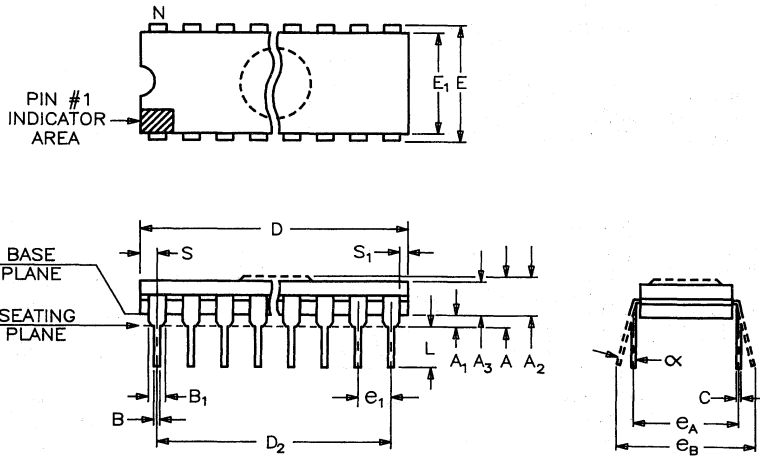
32 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A ₁	0.38			0.015		
A ₂	3.56	4.95		0.140	0.195	
A ₃	3.56	4.70		0.140	0.185	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	41.66	42.67		1.640	1.680	
D ₂	41.91		Reference	1.650		Reference
E	15.24	15.75		0.600	0.620	
E ₁	14.48	15.37		0.570	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	15.49		Reference	0.610		Reference
e _B	15.75	17.78		0.620	0.700	
L	3.18	4.32		0.125	0.170	
N	32			32		
S	1.40	2.29		0.055	0.090	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

40 LEAD CERDIP DUAL IN-LINE PACKAGE

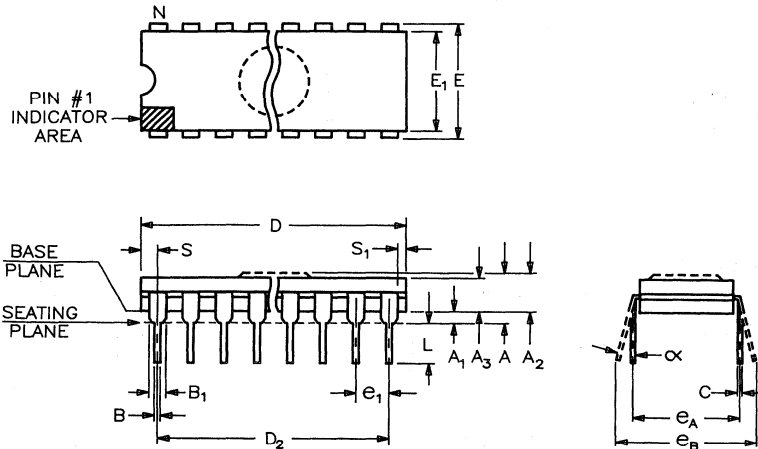


231369-29

2

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A ₁	0.38			0.015		
A ₂	3.56	4.95		0.140	0.195	
A ₃	3.56	4.70		0.140	0.185	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30		0.009	0.012	
D	51.69	52.96		2.035	2.085	
D ₂	48.26		Reference	1.900		Reference
E	15.24	15.75		0.600	0.620	
E ₁	13.08	15.37		0.515	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	15.49		Reference	0.610		Reference
e _B	15.75	17.78		0.620	0.700	
L	3.18	4.32		0.125	0.170	
N	40			40		
S	1.40	2.29		0.055	0.090	
S ₁	0.13			0.005		
ISSUE	IWS 10/12/88					

42 LEAD CERDIP DUAL IN-LINE PACKAGE



231369-29

Family: Cerdip Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.72			0.225	
A ₁	0.38			0.015		
A ₂	3.56	4.95		0.140	0.195	
A ₃	3.56	4.70		0.140	0.185	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30		0.009	0.012	
D	54.23	55.50		2.135	2.185	
D ₂	50.80		Reference	2.000		Reference
E	15.24	15.75		0.600	0.620	
E ₁	13.08	15.37		0.515	0.605	
e ₁	2.29	2.79		0.090	0.110	
e _A	15.49		Reference	0.610		Reference
e _B	15.75	17.78		0.620	0.700	
L	3.18	4.32		0.125	0.170	
N	42			42		
S	1.40	2.29		0.055	0.090	
S ₁	0.13			0.005		
ISSUE	IWS 9/19/90					



CERQUAD PACKAGE

Symbol List for Cerquad Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A ₁	Shoulder to Board Height
C	Lead Thickness
CP	Seating Plane Coplanarity
D	Outside Dimension
D ₁	Ceramic Body Dimension
D ₂	Footprint
D ₃	Footprint
E	Outside Dimension
E ₁	Ceramic Body Dimension
E ₂	Footprint
E ₃	Footprint
N	No. of Leads

2

NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. To be determined at seating plane —E—.
3. Dimensions D1 and E1 do not include glass protrusion.
4. Controlling dimension, inch.
5. All dimensions and tolerances include lead trim offset and lead plating finish.

Packaging Family Attributes	
Category	Cerquad
Acronym	Cerquad
Lead Configuration	Quad
Lead Counts	44, 52, 68
Lead Finish	SolderCoat
Lead Pitch	0.050"
Board Assembly Type	Socket
Standard Registration	JEDEC

NOTES:

1. Alloy 42 - "J" Leads.
2. Pressed Ceramic Body.
3. UV Window available for reprogramming.
4. Compatible with PLCC Footprint.
5. Not certified for Surface Mount, must be Socketed.

CERQUAD PACKAGE (SQUARE)

Family: 44 Lead Cerquad Square						
Symbol	Millimeters		Inches			Notes
	Min	Max	Min	Max	Nominal	
A	3.94	4.57	0.155	0.180		
A ₁	2.29	3.05	0.090	0.120	0.100	
C	0.15	0.25	0.006	0.010	0.007	
CP	0.00	0.15	0.000	0.006		
D	17.40	17.65	0.685	0.695	0.690	
D ₁	16.00	16.66	0.630	0.656	0.650	(Note 3)
D ₂	15.24	15.75	0.590	0.630	0.620	(Note 2)
D ₃	12.70		0.500			Reference
E	17.40	17.65	0.685	0.695	0.690	
E ₁	16.36	16.66	0.635	0.656	0.650	(Note 3)
E ₂	15.24	15.75	0.590	0.630	0.620	(Note 2)
E ₃	12.70		0.500			Reference
N	44		44			
Issue	IWS 04/19/90					

CERQUAD PACKAGE (SQUARE)

Family: 52 Lead Cerquad Square						
Symbol	Millimeters		Inches			Notes
	Min	Max	Min	Max	Nominal	
A	4.20	4.83	0.165	0.190		
A ₁	2.29	3.30	0.090	0.130	0.100	
C	0.15	0.25	0.006	0.010	0.007	
CP	0.00	0.15	0.000	0.006		
D	19.94	20.19	0.785	0.795	0.790	
D ₁	18.542	19.202	0.730	0.756	0.750	(Note 3)
D ₂	17.53	18.54	0.690	0.730	0.720	(Note 2)
D ₃	15.24		0.600			Reference
E	19.94	20.19	0.785	0.795	0.790	
E ₁	18.669	19.202	0.735	0.756	0.750	(Note 3)
E ₂	17.53	18.54	0.690	0.730	0.720	(Note 2)
E ₃	15.24		0.600			Reference
N	52		52			
Issue	IWS 04/19/90					

2

Family: 68 Lead Cerquad Square						
Symbol	Millimeters		Inches			Notes
	Min	Max	Min	Max	Nominal	
A	3.94	4.83	0.155	0.190		
A ₁	2.29	3.05	0.090	0.120	0.100	
C	0.15	0.25	0.006	0.010	0.007	
CP	0.00	0.15	0.000	0.006		
D	25.02	25.27	0.985	0.995	0.990	
D ₁	23.62	24.33	0.930	0.958	0.950	(Note 3)
D ₂	22.86	23.37	0.890	0.930	0.920	(Note 2)
D ₃	20.32		0.800			Reference
E	25.02	25.27	0.985	0.995	0.990	
E ₁	23.93	24.33	0.935	0.958	0.950	(Note 3)
E ₂	22.86	23.37	0.890	0.930	0.920	(Note 2)
E ₃	20.32		0.800			Reference
N	68		68			
Issue	IWS 07/19/90					

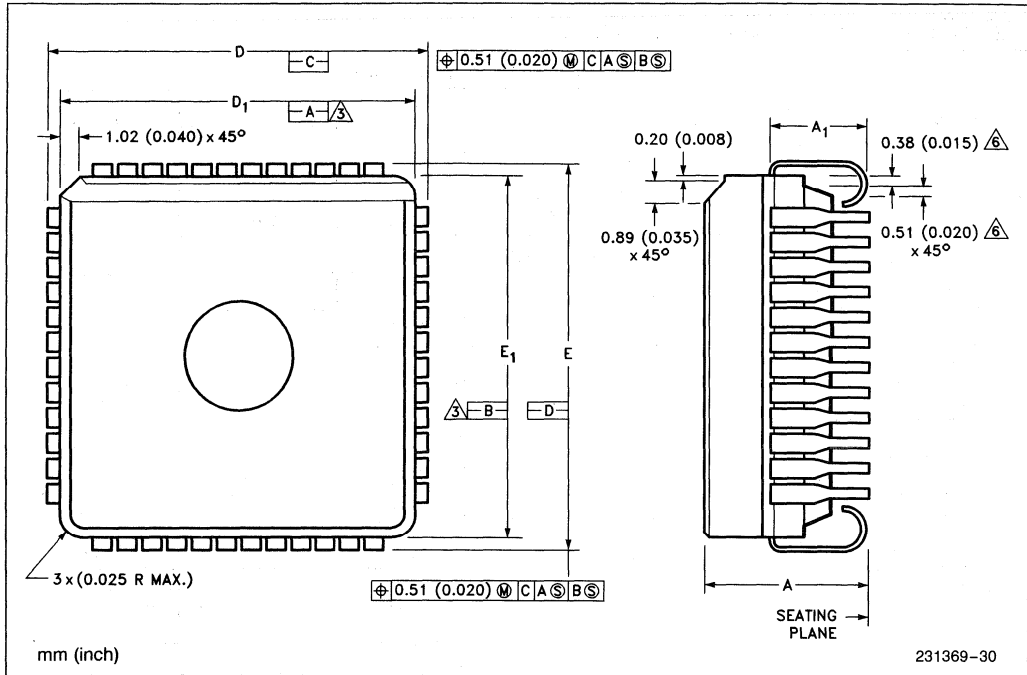


Figure 1. Principal Dimensions and Datums

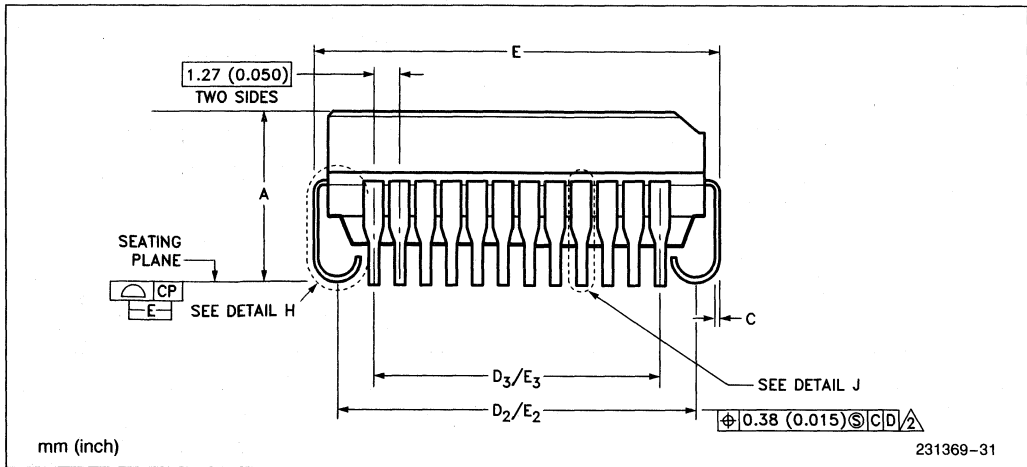
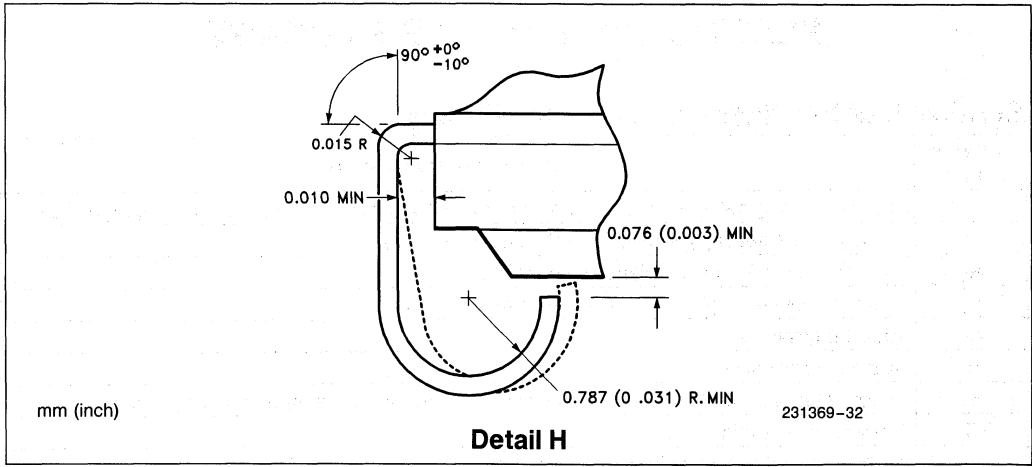
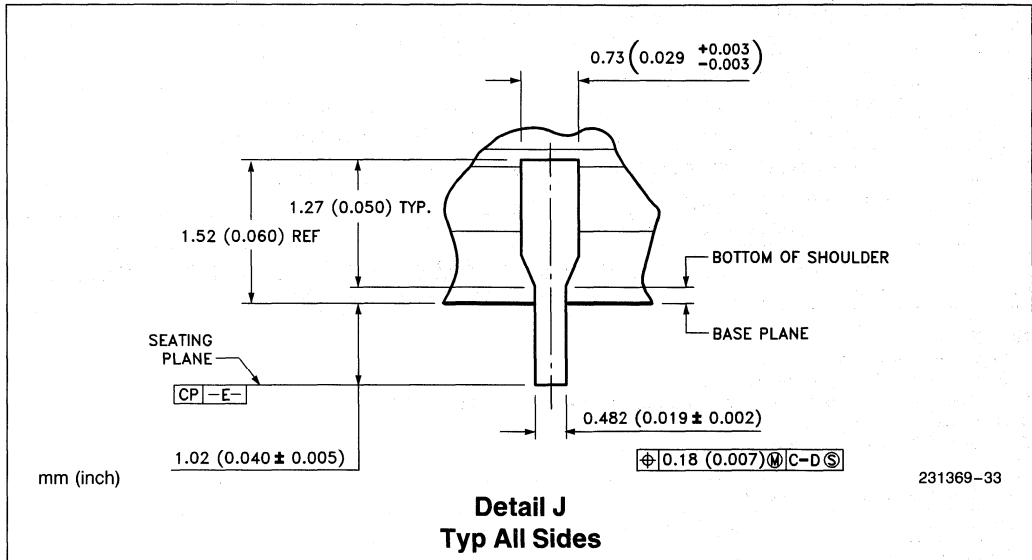


Figure 2. Terminal Details



2





PLASTIC DUAL IN-LINE PACKAGE

Symbol List for Plastic Dual In-Line Family

Letter or Symbol	Description of Dimensions
α	Angular spacing between minimum and maximum lead positions measured at the gauge plane
A	Distance from seating plane to highest point of body (lid)
A ₁	Distance between seating plane and base plane
A ₂	Distance from base plane to highest point of body (lid)
A ₃	Base body thickness
B	Width of terminal leads
B ₁	Width of terminal lead shoulder which locates seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package dimension of length
D ₂	A body length dimension, end lead center to end lead center
E	Largest overall package width dimension outside of lead
E ₁	Body width dimensions not including leads
e _A	Linear spacing of true minimum lead position center line to center line
e _B	Linear spacing between true lead position outside of lead to outside of lead
e ₁	Linear spacing between centerlines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	The total number of potentially useable lead positions
S	Distance from true position centerline of No. 1 lead position to the extremity of the body
S ₁	Distance from other end lead edge positions to the extremity of the body

NOTES:

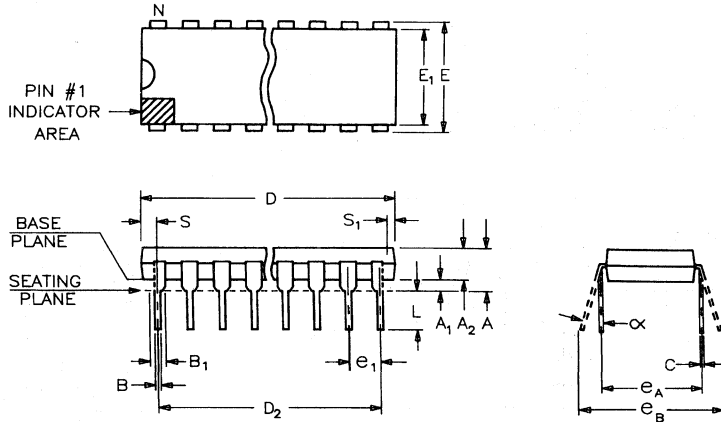
1. Controlling dimension: millimeter.
2. Dimension "e₁" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimension "B₁" is nominal.
5. Details of Pin 1 identifier are optional.

Packaging Family Attributes	
Category	Plastic Dual-In-Line
Acronym	PDIP
Lead Configuration	Dual-In-Line
Lead Counts	16, 18, 20, 24, 28, 32, 40, 48, 64
Lead Finish	SolderCoat
Lead Pitch	0.100"
Board Assembly Type	Socket and Insertion Mount
Standard Registration	JEDEC and EIAJ

NOTES:

1. Alloy 42 and Cu Alloy Leads.
2. Novalac Body.

16 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: 1/2 LEAD

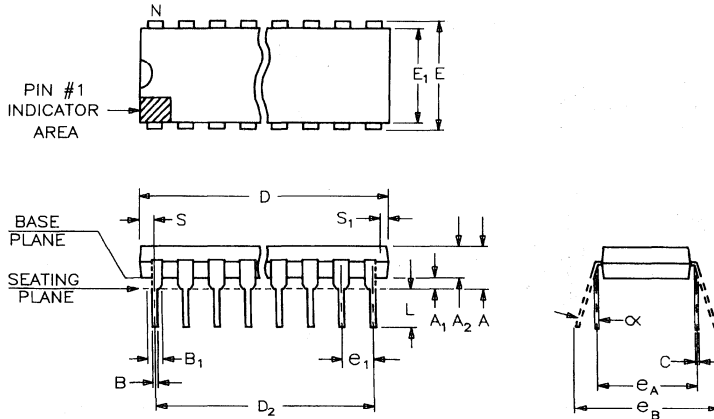


231369-34

2

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.18	3.56		0.125	0.140	
B	0.41	0.53		0.016	0.021	
B ₁	1.52		Typical	0.060		Typical
C	0.20	0.36	Typical	0.008	0.014	Typical
D	18.78	19.81		0.74	0.780	
D ₂	17.78		Reference	0.700		Reference
E		8.13			0.320	
E ₁	6.10	6.60		0.240	0.260	
e ₁	2.29	2.79	Typical	0.090	0.110	Typical
e _A	7.37		Reference	0.290		Reference
e _B	7.62	10.16		0.300	0.400	
L	3.05	3.68		0.120	0.145	
N	16		1/2 Lead	16		1/2 Lead
S	0.51	1.02		0.020	0.040	
S ₁	0.23			0.009		
ISSUE	IWS	4/19/90				

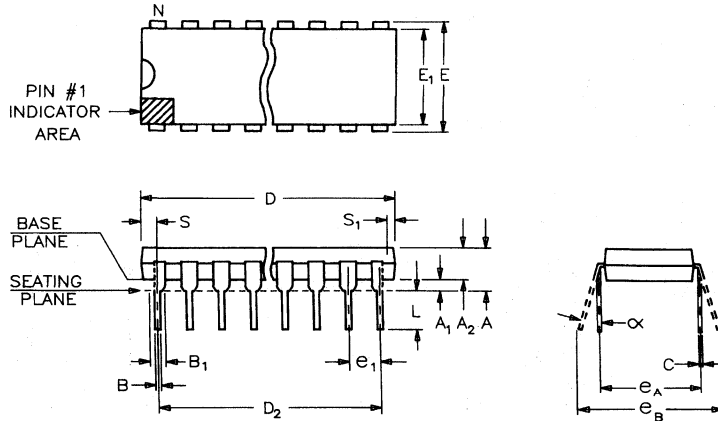
16 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: 1/2 LEAD/WIDEBODY



231369-34

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.18	3.61		0.125	0.142	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	19.18	19.81		0.755	0.780	
D ₂	17.78		Reference	0.700		Reference
E		8.13			0.320	
E ₁	6.73	6.99		0.265	0.275	
e ₁	2.29			0.090	0.110	
e _A	7.37		Reference	0.290		Reference
e _B	7.62	10.16		0.300	0.400	
L	3.05	3.68		0.120	0.145	
N	16		1/2 Lead/Widebody	16		1/2 Lead/Widebody
S	0.51	1.02		0.020	0.040	
S ₁	0.23			0.009		
ISSUE	IWS 4/19/90					

18 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: 1/2 LEAD

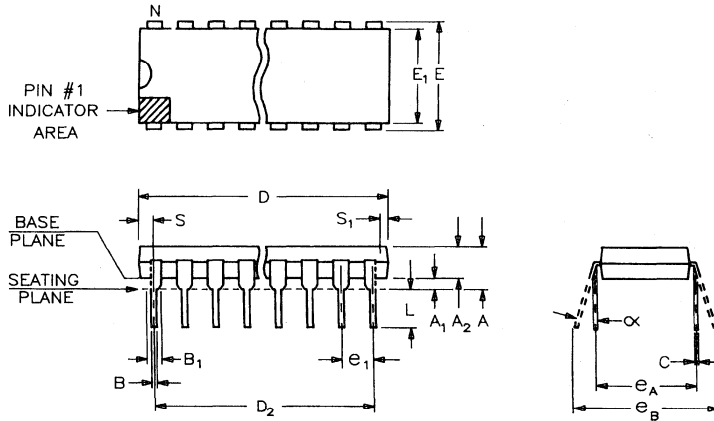


231369-34

2

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.57	4.57		0.140	0.180	
A ₁	0.51			0.020		
A ₂	3.06	4.06		0.120	0.160	
B	0.36	0.56		0.014	0.022	
B ₁	1.27		Typical	0.050		Typical
C	0.20	0.30		0.008	0.012	
D	22.83	23.09		0.899	0.909	
D ₂						
E	8.13		Typical	0.320		Typical
E ₁	6.27	6.53		0.247	0.257	
e ₁	2.54		Typical	0.100		Typical
e _A	7.62		Typical	0.300		Typical
e _B						
L	3.05			0.120		
N	18		1/2 Lead	18		1/2 Lead
S						
S ₁						
ISSUE	IWS	4/19/90				

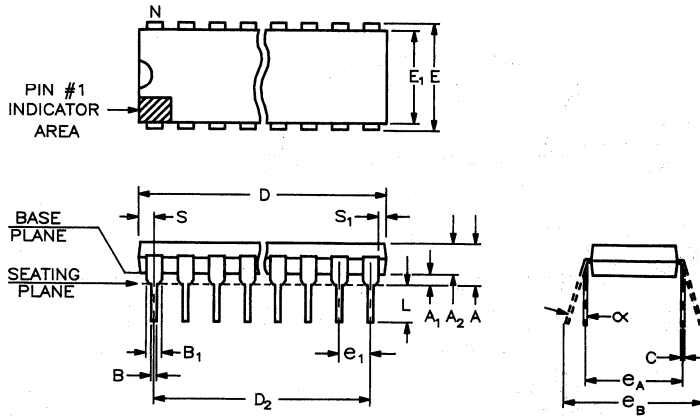
**18 LEAD PLASTIC DUAL IN-LINE PACKAGE
VARIATION: 1/2 LEAD/WIDEBODY**



231369-34

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.004			0.197	
A ₁	0.51			0.020		
A ₂	3.43	3.68		0.135	0.145	
B	0.41	0.58		0.016	0.023	
B ₁	1.19	1.49		0.047	0.065	
C	0.20	0.30		0.008	0.012	
D	21.84	22.37		0.860	0.875	
D ₂						
E	7.62		Typical	0.300		Typical
E ₁		7.37			0.290	
e ₁	2.54			0.100		Typical
e _A						
e _B						
L	3.00	3.68		0.118		
N	18		Widebody	18		Widebody
S						
S ₁						
ISSUE	IWS	4/19/90				

18 LEAD PLASTIC DUAL IN-LINE PACKAGE

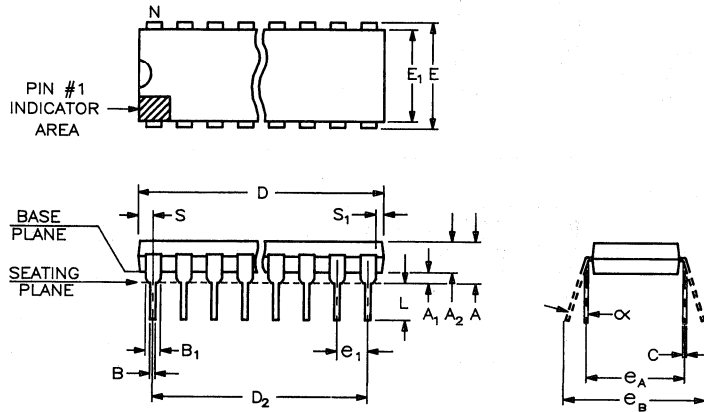


231369-35

2

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	5°		0°	5°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.18	3.68		0.125	0.145	
B	0.41	0.53		0.016	0.021	
B ₁	1.52		Typical	0.060		Typical
C	0.20	0.36	Typical	0.008	0.014	Typical
D	21.34	23.37		0.240	0.920	
D ₂	20.32		Reference	0.800		Reference
E		8.26			0.320	
E ₁	6.10	7.37		0.240	0.290	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.66		Reference	0.290		Reference
e _B	7.62	10.16		0.300	0.400	
L	3.05	3.68		0.120	0.145	
N	18			18		
S	1.02	1.52		0.040	0.060	
S ₁	0.23			0.009		
ISSUE	IWS	4/19/90				

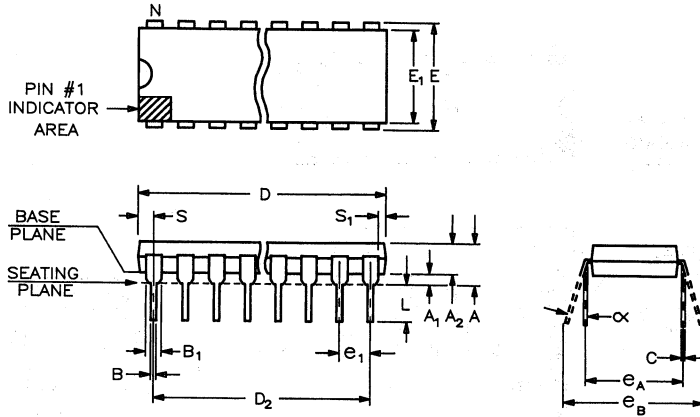
18 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: WIDEBODY



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.18	3.56		0.125	0.140	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	22.73	23.37		0.895	0.920	
D ₂	20.32		Reference	0.800		Reference
E		8.13			0.320	
E ₁	6.73	6.98		0.265	0.275	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.37		Reference	0.290		Reference
e _B	7.62	10.16		0.300	0.400	
L	3.18	3.68		0.125	0.145	
N	18		Widebody	18		Widebody
S	1.02	1.52		0.040	0.060	
S ₁	0.23			0.009		
ISSUE	IWS 10/12/88					

20 LEAD PLASTIC DUAL IN-LINE PACKAGE

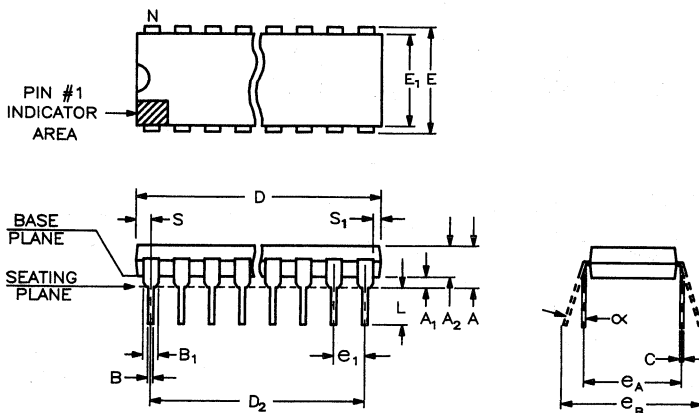


231369-35

2

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.18	3.68		0.125	0.145	
B	0.41	0.58		0.016	0.023	
B ₁	1.19	1.52		0.047	0.060	
C	0.20	0.30		0.008	0.012	
D	24.43	26.67		0.962	1.050	
D ₂	22.86		Reference	0.900		Reference
E	7.62	8.13		0.300	0.320	
E ₁	6.22	6.48		0.245	0.255	
e ₁	2.29	2.79		0.090	0.110	
e _A	7.37		Reference	0.290		Reference
e _B	7.62	10.16		0.300	0.400	
L	3.00	3.68		0.118	0.145	
N	20			20		
S	1.40	1.91		0.055	0.075	
S ₁	0.61			0.024		
ISSUE	IWS 10/12/88					

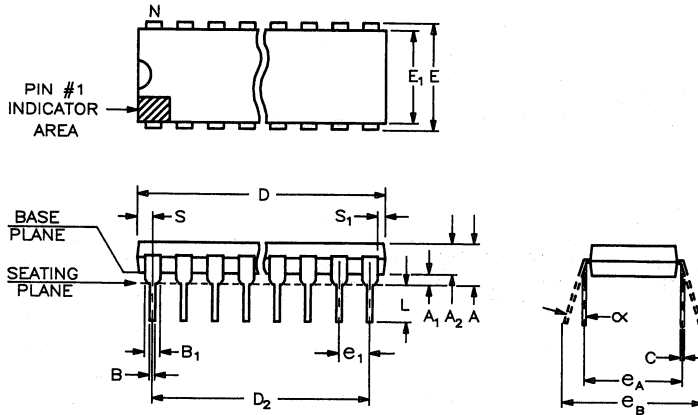
24 LEAD PLASTIC DUAL IN-LINE PACKAGE (300 MIL) VARIATION: SKINNY DIP



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A		4.32			0.170	
A ₁	0.38			0.015		
A ₂	3.18	3.65		0.130		
B	0.41	0.51		0.016	0.020	
B ₁	1.40	1.65		0.055	0.065	
C	0.20	0.30		0.008	0.012	
D	31.34	31.88		1.245	1.255	
D ₂	27.94		Reference	1.100		Reference
E	7.62	8.26		0.300	0.325	
E ₁	6.35	8.26		0.250	0.325	
e ₁	2.54		Reference	0.100		Reference
e _A	7.62		Reference	0.300		Reference
e _B	7.62	10.16		0.300	0.400	
L	3.05	3.68		0.120	0.145	
N	24		300 MIL	24		300 MIL
S	1.78	2.03		0.070	0.080	
S ₁	1.02			0.040		
ISSUE	IWS	4/19/90				

24 LEAD PLASTIC DUAL IN-LINE PACKAGE (600 MIL)

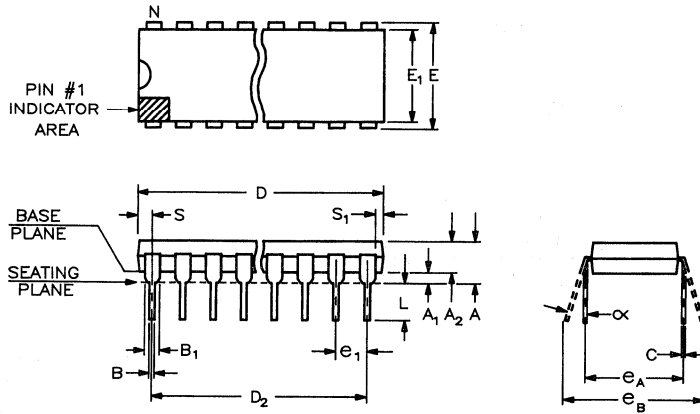


231369-35

2

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.68	4.06		0.145	0.160	
B	0.41	0.51		0.016	0.020	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	31.37	32.00		1.235	1.260	
D ₂	27.94		Reference	1.100		Reference
E		15.75			0.620	
E ₁	13.59	13.84		0.535	0.545	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	17.78		0.600	0.700	
L	3.18	3.68		0.125	0.145	
N	24			24		
S	1.52	2.03		0.060	0.080	
S ₁	0.74			0.029		
ISSUE	IWS	4/19/90				

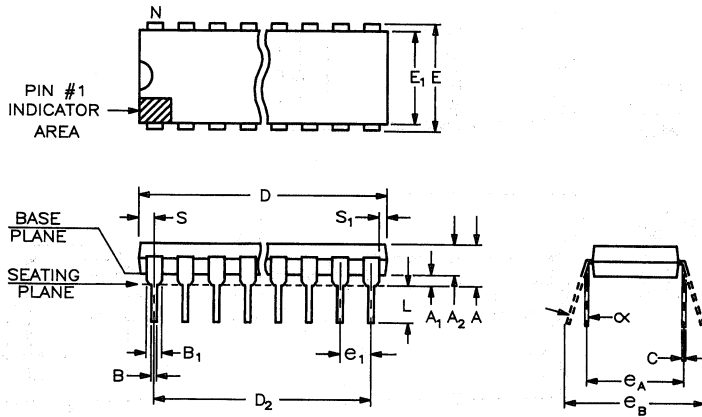
28 LEAD PLASTIC DUAL IN-LINE PACKAGE (300 MIL)



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A		4.32			0.170	
A ₁	0.38			0.015		
A ₂	3.30		Typical	0.130		Typical
B	0.41	0.51		0.016	0.020	
B ₁	1.14	1.40		0.045	0.055	
C	0.20	0.30		0.008	0.012	
D	34.16	34.42		1.345	1.355	
D ₂	33.02		Reference	1.300		Reference
E	7.62	8.62		0.300	0.339	
E ₁	6.86	7.37		0.270	0.290	
e ₁	2.54		Reference	0.100		Reference
e _A	7.62		Reference	0.300		Reference
e _B	7.62	10.16		0.300	0.400	
L	3.18	3.43		0.125	0.135	
N	28		300 MIL	28		300 MIL
S	0.051	0.76		0.020	0.030	
S ₁	0.23			0.009		
ISSUE	IWS	4/19/90				

28 LEAD PLASTIC DUAL IN-LINE PACKAGE (600 MIL)

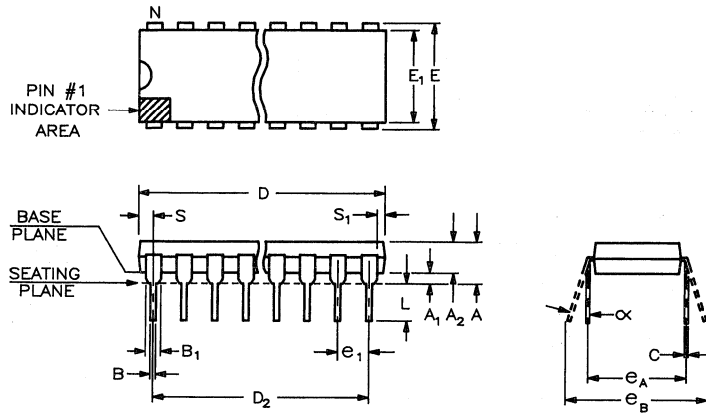


231369-35

2

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.68	4.06		0.145	0.160	
B	0.36	0.56		0.014	0.022	
B ₁	1.52		Typical	0.060		Typical
C	0.23	0.30		0.009	0.012	
D	36.70	37.34		1.445	1.470	
D ₂	33.02		Reference	1.300		Reference
E		15.75			0.620	
E ₁	13.59	14.0		0.535	0.551	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	17.78		0.600	0.700	
L	3.18	3.68		0.125	0.145	
N	28		600 MIL	28		600 MIL
S	1.65	2.16		0.065	0.085	
S ₁	0.86			0.034		
ISSUE	IWS	4/19/90				

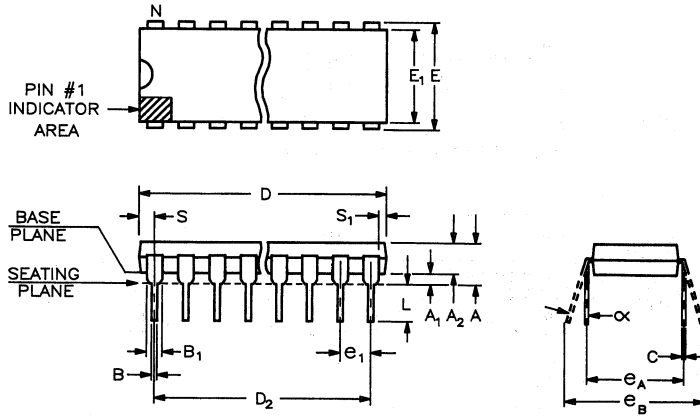
32 LEAD PLASTIC DUAL IN-LINE PACKAGE (600 MIL)



231369-35

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A		4.83			0.190	
A ₁	0.38			0.015		
A ₂	3.81		Typical	0.150		Typical
B	0.41	0.51		0.016	0.020	
B ₁	1.14	1.40		0.045	0.055	
C	0.20	0.30		0.008	0.012	
D	41.78	42.04		1.645	1.655	
D ₂	38.10		Reference	1.500		Reference
E	15.24	15.88		0.600	0.625	
E ₁	13.46	13.97		0.530	0.550	
e ₁	2.54		Reference	0.100		Reference
e _A	15.24		Reference	0.600		Reference
e _B	15.24	17.78		0.600	0.700	
L	3.18	3.43		0.125	0.135	
N	32		600 MIL	32		600 MIL
S	1.78	2.03		0.070	0.080	
S ₁	1.14			0.045		
ISSUE	IWS	4/19/90				

40 LEAD PLASTIC DUAL IN-LINE PACKAGE

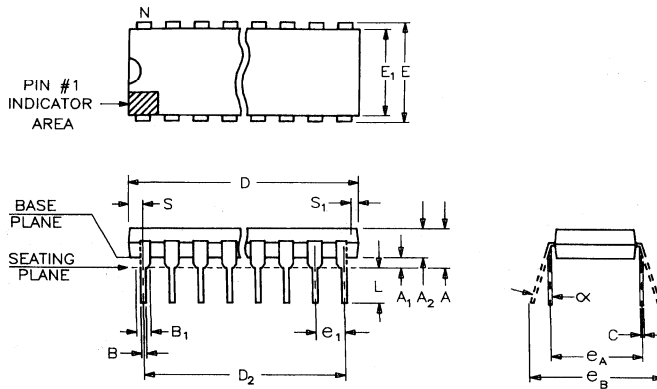


231369-35

2

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.94	4.19		0.155	0.165	
B	0.41	0.51		0.016	0.020	
B ₁	1.27		Typical	0.050		Typical
C	0.23	0.30		0.009	0.012	
D	51.94	52.58		2.045	2.070	
D ₂	48.26		Reference	1.900		Reference
E		15.75			0.620	
E ₁	13.59	13.84		0.535	0.545	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	17.78		0.600	0.700	
L	3.18	3.68		0.125	0.145	
N	40			40		
S	1.65	2.16		0.065	0.085	
S ₁	0.99			0.039		
ISSUE	IWS 4/19/90					

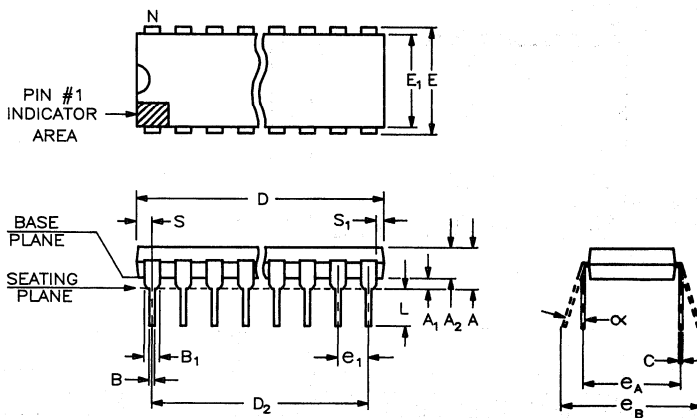
40 LEAD PLASTIC DUAL IN-LINE PACKAGE VARIATION: 1/2 LEAD



231369-34

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
a	0°	10°		0°	10°	
A	4.55			0.179		
A ₁	0.38			0.015		
A ₂	3.75	3.95	Nom 3.85	0.147	0.155	
B	0.35	0.51		0.014	0.020	
B ₁	1.4	1.6		0.055	0.063	
C	0.25	0.45	Nom 0.35	0.009	0.018	
D		52.3			2.06	
D ₂						
E	13.5	13.9	Nom 13.7	0.531	0.547	
E ₁						
e ₁	2.29	2.79	Nom 2.54	0.090	0.110	
e _A	14.74	15.74	Nom 15.24	0.580	0.619	
e _B						
L	3.0	3.6	Nom 3.3	0.118	0.141	
N	40		1/2 Lead	40		1/2 Lead
S	1.65	2.16		0.065	0.080	
S ₁						
ISSUE	IWS	4/19/90				

48 LEAD PLASTIC DUAL IN-LINE PACKAGE

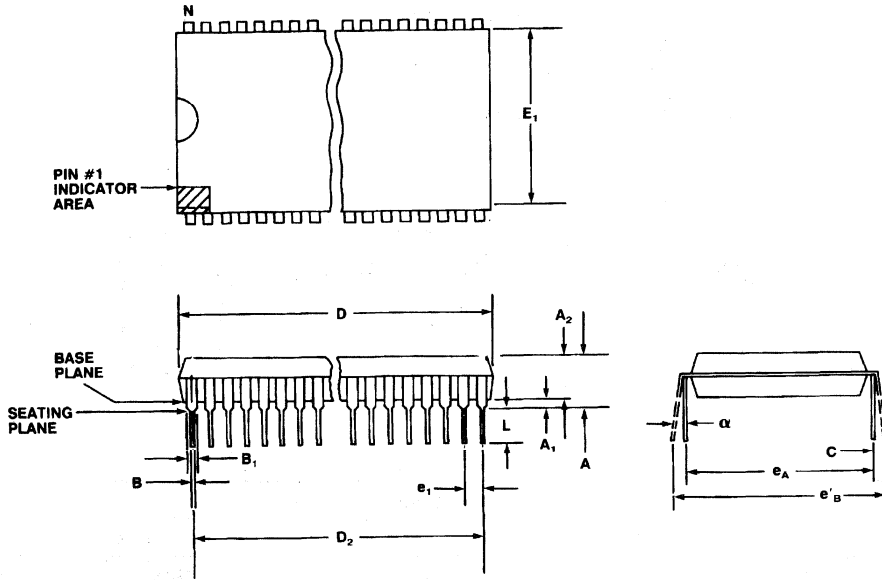


231369-35

2

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A ₁	0.38			0.015		
A ₂	3.94	4.32		0.155	0.170	
B	0.41	0.51		0.016	0.020	
B ₁	1.27		Typical	0.050		Typical
C	0.23	0.30		0.009	0.012	
D	61.60	61.98		2.425	2.440	
D ₂	58.42		Reference	2.300		Reference
E		15.75			0.620	
E ₁	13.84	14.10		0.545	0.555	
e ₁	2.29	2.79		0.090	0.110	
e _A	14.99		Reference	0.590		Reference
e _B	15.24	17.78		0.600	0.700	
L	3.18	3.68		0.125	0.145	
N	48			48		
S	1.65	2.16		0.065	0.085	
S ₁	0.99	1.40		0.039	0.055	
ISSUE	IWS 4/19/90					

64 LEAD PLASTIC DUAL IN-LINE PACKAGE (SHRINK)



231369-36

Family: Plastic Dual In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A		5.65			0.22	
A ₁	0.51			0.020		
A ₂	4.15	4.35		0.163	0.171	
B	0.35	0.55		0.014	0.022	
B ₁	1.0		Typical	0.040		Typical
C	0.20	0.30		0.008	0.012	
D	57.8	58.2		2.28	2.29	
D ₂	55.12		Reference	2.170		Reference
E						
E ₁	16.8	17.2		0.661	0.677	
e ₁	1.60	1.96		0.063	0.077	
e _A	19.05			0.745 BSC		
e _B	19.5	21.0		0.767	0.826	
L	3.0	3.6		0.118	0.142	
N	64			64		
ISSUE	9/19/90					



PLASTIC FLATPACK PACKAGE

Symbol List for Plastic Flatpack Family

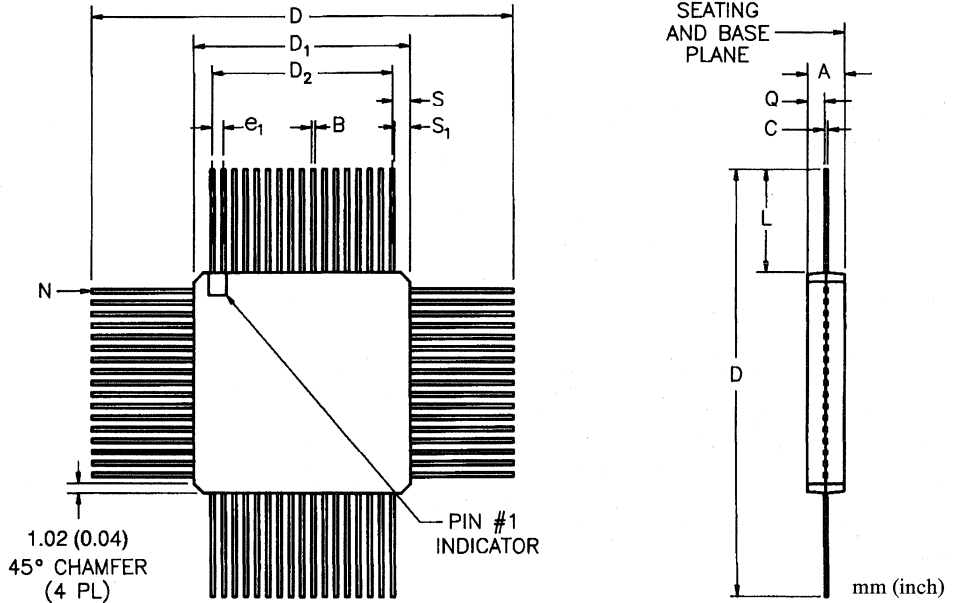
Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package dimension of length
D ₁	Largest overall package dimension of length excluding leads
D ₂	A body length dimension, outer lead center to outer lead center
e ₁	Linear spacing between centerlines of terminal leads
L	Lead dimension free lead length
N	The total number of potentially useable lead positions
Q	Lead plane to top of body plane distance
S	Distance from true position centerline of end lead position to the extremity of the body
S ₁	Linear spacing of true maximum lead position from lead edge to package edge

NOTES:

1. Controlling dimension: millimeter.
2. Dimension "e₁" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions "B", "B₁" and "C" are nominal.

2

68 LEAD PLASTIC FLATPACK PACKAGE



231369-37

Family: Plastic Flatpack Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	4.19	4.34		0.165	0.171	
B	0.46	0.56		0.018	0.022	Typical
C	0.18	0.25		0.007	0.010	Typical
D	44.45	45.21		1.750	1.780	
D ₁	24.08	24.26		0.948	0.955	
D ₂	20.22	20.42		0.796	0.804	
e ₁	1.22	1.32	Typical	0.048	0.052	Typical
L	10.16	10.80		0.400	0.425	
N	68			68		
Q	2.01	2.06		0.079	0.081	
S	1.73	2.08		0.068	0.082	
S ₁	1.47			0.058		
ISSUE	IWS 10/12/88					



PLASTIC LEADED CHIP CARRIER PACKAGE

Symbol List for Plastic Leaded Chip Carrier Family

Letter or Symbol	Description of Dimensions
A	Overall Height: Distance from seating plane to highest point of body
A1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Overall package dimension
D1/E1	Plastic body dimension
D2/E2	Footprint
LT	Lead thickness
N	Total number of leads
Nd	Total number of leads on short side
Ne	Total number of leads on long side
TCP	Tweezing coplanarity

2

NOTES RECTANGLE PACKAGE:

- All dimensions and tolerances conform to ANSI Y14.5M-1982.
- Datum plane **H** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
- Datums **A-B** and **D** to be determined where center leads exit plastic body at datum plane **H**.
- To be determined at seating plane **C**.
- Dimensions D1 and E1 do not include mold protrusion.
- Pin 1 identifier is located within the defined zone.
- These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
- Nd denotes the number of leads on the two short sides of the package, one of which contains pin #1. Ne denotes the number of leads on the two long sides of the package.
- Controlling dimension, inch.
- All dimensions and tolerances include lead trim offset and lead plating finish.
- Tweezing surface planarity is defined as the furthest any lead on a side may be from the datum. The datum is established by touching the outermost lead on that side and parallel to **A-B** or **D**.

Packaging Family Attributes	
Category	Plastic Leaded Chip Carrier
Acronym	PLCCC
Lead Configuration	Quad
Lead Counts	28, 32, 44, 52, 68, 84
Lead Finish	SolderPlate
Lead Pitch	0.050"
Board Assembly Type	Socket and Surface Mount
Standard Registration	JEDEC and EIAJ

NOTES:

- Copper Alloy Leads.
- Novalac Body.
- Bake and dessicant packaging required.



PACKAGE/MODULE OUTLINES AND DIMENSIONS

Family: Plastic Leaded Chip Carrier-Rectangular (mm)						
Symbol	28 Lead			32 Lead		
	Min	Max	Notes	Min	Max	Notes
A	3.20	3.56		3.20	3.56	
A ₁	1.93	2.29		1.93	2.29	
D	9.78	10.0		12.3	12.6	
D ₁	8.81	8.97		11.4	11.5	
D ₂	7.37	8.38		9.91	10.9	
E	14.9	15.1		14.9	15.1	
E ₁	13.9	14.0		13.9	14.0	
E ₂	12.4	13.5		12.4	13.5	
N	28			32		
N _d	5			7		
N _e	9			9		
CP	0.00	0.10		0.00	0.10	
TCP	0.00	0.10		0.00	0.10	
LT	0.23	0.38		0.23	0.38	
ISSUE	IWS 10/12/88					

Family: Plastic Leaded Chip Carrier-Rectangular (inch)						
Symbol	28 Lead			32 Lead		
	Min	Max	Notes	Min	Max	Notes
A	0.126	0.140		0.126	0.140	
A ₁	0.076	0.090		0.076	0.090	
D	0.385	0.395		0.485	0.495	
D ₁	0.347	0.353		0.447	0.453	
D ₂	0.290	0.330		0.390	0.430	
E	0.585	0.595		0.585	0.595	
E ₁	0.547	0.553		0.547	0.553	
E ₂	0.490	0.530		0.490	0.530	
N	28			32		
N _d	5			7		
N _e	9			9		
CP	0.000	0.004		0.000	0.004	
TCP	0.000	0.004		0.000	0.004	
LT	0.009	0.015		0.009	0.015	
ISSUE	IWS 10/12/88					

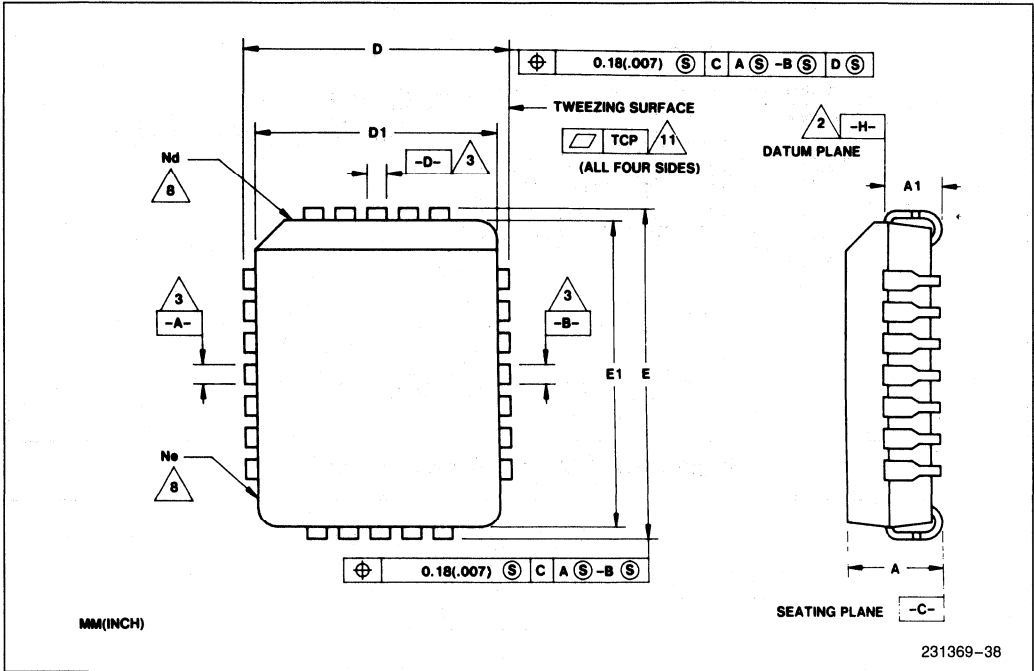


Figure 1. Principal Dimensions and Datums

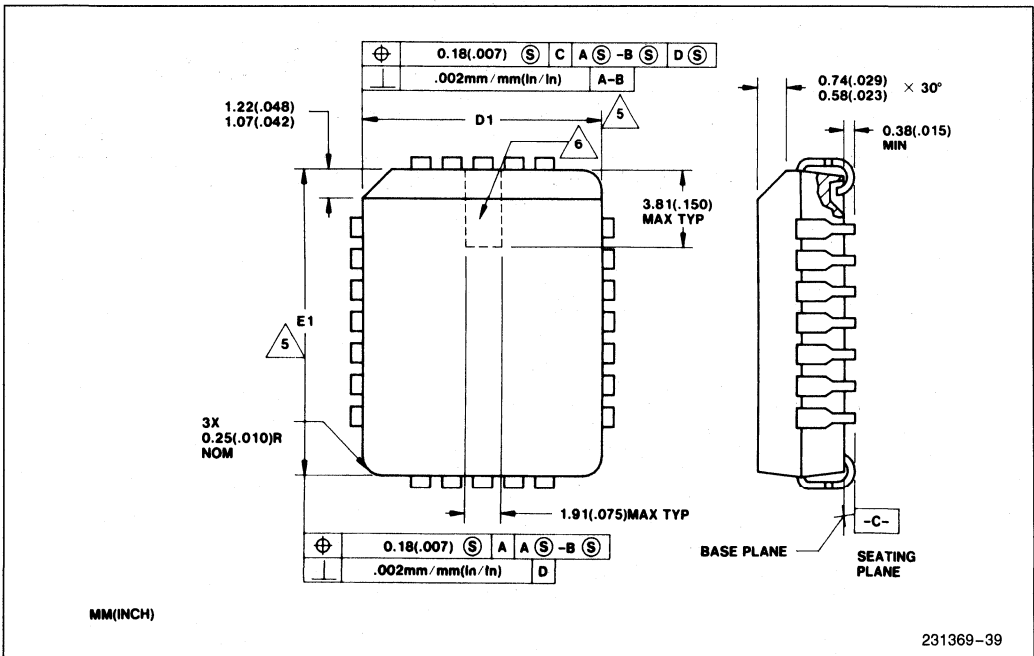


Figure 2. Molded Details

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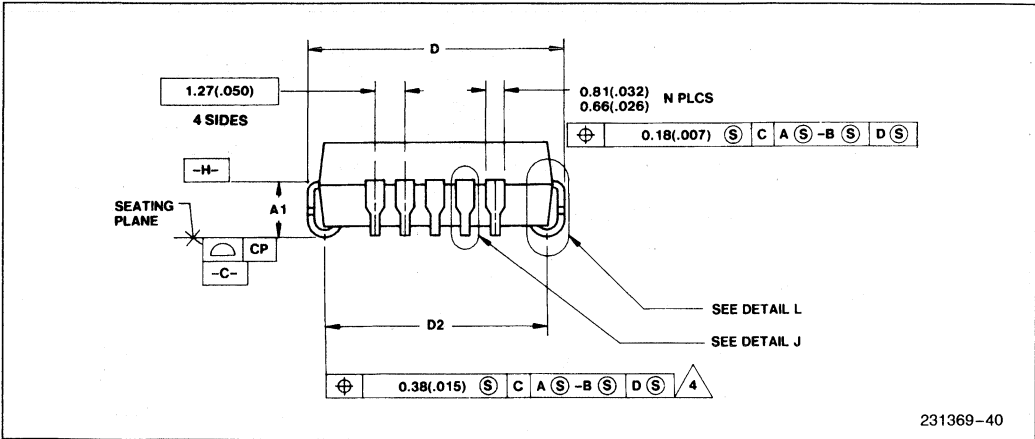


Figure 3A. Terminal Details N_D Side

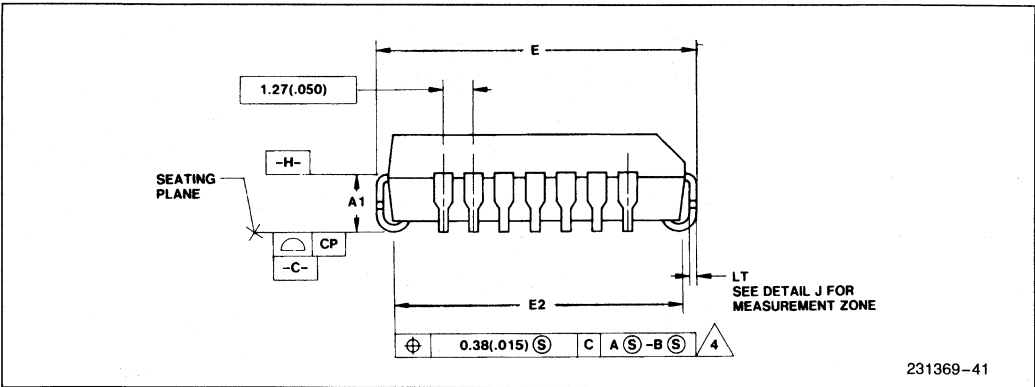
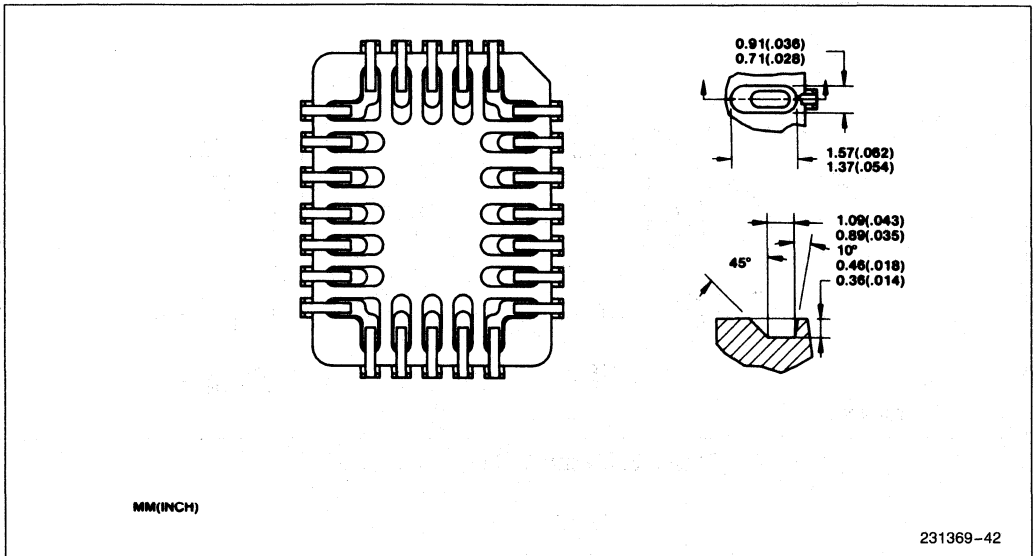


Figure 3B. Terminal Details N_E Side



2

Figure 4. Standard Package Bottom View

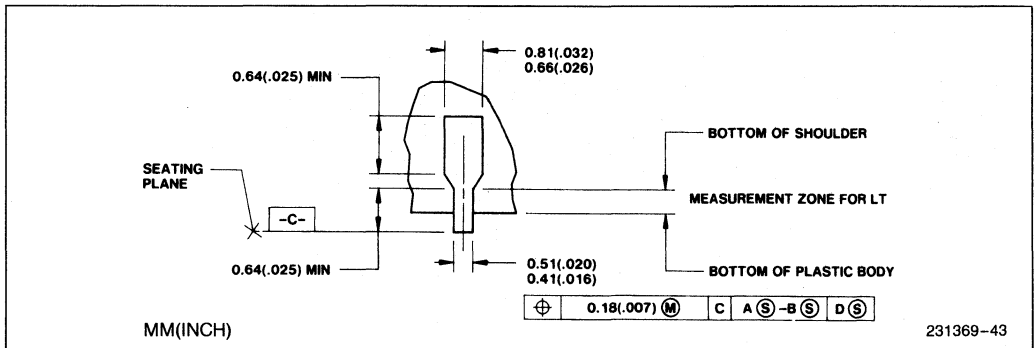


Figure 5. Detail J. Terminal Details

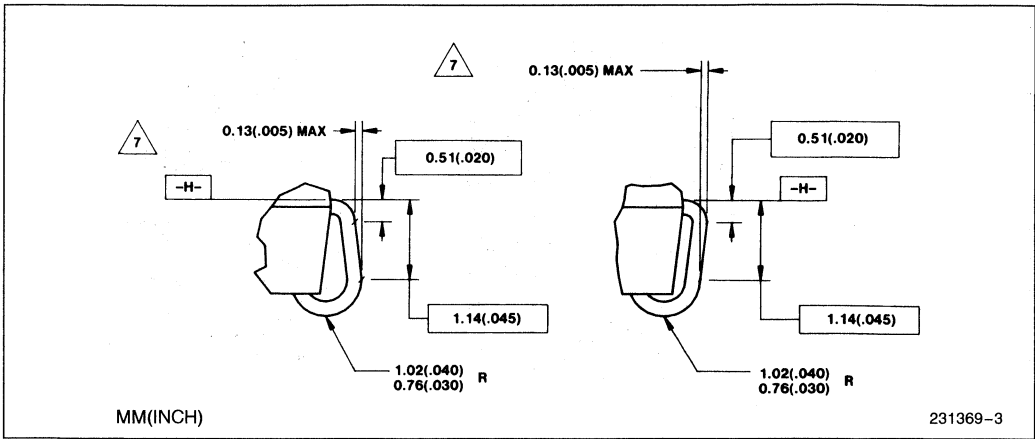


Figure 7. Detail L. Terminal Details



PACKAGE/MODULE OUTLINES AND DIMENSIONS

Family: Plastic Leaded Chip Carrier-Square (mm)									
Symbol	20 Lead			28 Lead			44 Lead		
	Min	Max	Notes	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		4.19	4.57		4.19	4.57	
A ₁	2.29	3.05		2.29	3.05		2.29	3.05	
D	9.78	10.0		12.3	12.6		17.4	17.7	
D ₁	8.89	9.04		11.4	11.6		16.5	16.7	
D ₂	7.37	8.38		9.91	10.9		15.0	16.0	
E	9.78	10.0		12.3	12.6		17.4	17.7	
E ₁	8.89	9.04		11.4	11.6		16.5	16.7	
E ₂	7.37	8.38		9.91	10.9		15.0	16.0	
N	20			28			44		
CP	0.00	0.10		0.00	0.10		0.00	0.10	
TCP	0.00	0.10		0.00	0.10		0.00	0.10	
LT	0.23	0.38		0.23	0.38		0.23	0.38	
ISSUE	IWS 10/12/88								

2

Family: Plastic Leaded Chip Carrier-Square (inch)									
Symbol	20 Lead			28 Lead			44 Lead		
	Min	Max	Notes	Min	Max	Notes	Min	Max	Notes
A	0.165	0.180		0.165	0.180		0.165	0.180	
A ₁	0.090	0.120		0.090	0.120		0.090	0.120	
D	0.385	0.395		0.485	0.495		0.685	0.695	
D ₁	0.350	0.356		0.450	0.456		0.650	0.656	
D ₂	0.290	0.330		0.390	0.430		0.590	0.630	
E	0.385	0.395		0.485	0.495		0.685	0.695	
E ₁	0.350	0.356		0.450	0.456		0.650	0.656	
E ₂	0.290	0.330		0.390	0.430		0.590	0.630	
N	20			28			44		
CP	0.000	0.004		0.000	0.004		0.000	0.004	
TCP	0.000	0.004		0.000	0.004		0.000	0.004	
LT	0.009	0.015		0.009	0.015		0.009	0.015	
ISSUE	IWS 10/12/88								



PACKAGE/MODULE OUTLINES AND DIMENSIONS

Family: Plastic Leaded Chip Carrier-Square (mm)									
Symbol	68 Lead			52 Lead			84 Lead		
	Min	Max	Notes	Min	Max	Notes	Min	Max	Notes
A	4.19	4.83		4.19	4.57		4.19	4.83	
A ₁	2.29	3.05		2.29	3.05		2.29	3.05	
D	25.0	25.3		19.9	20.2		30.1	30.4	
D ₁	24.1	24.3		19.1	19.2		29.2	29.4	
D ₂	22.6	23.6		17.5	18.5		27.7	28.7	
E	25.0	25.3		19.9	20.2		30.1	30.4	
E ₁	24.1	24.3		19.1	19.2		29.2	29.4	
E ₂	22.6	23.6		17.5	18.5		27.7	28.7	
N	68			52			84		
CP	0.00	0.10		0.00	0.10		0.00	0.10	
TCP	0.00	0.10		0.00	0.10		0.00	0.10	
LT	0.20	0.36		0.23	0.38		0.20	0.36	
ISSUE	IWS 10/12/88								

Family: Plastic Leaded Chip Carrier-Square (inch)									
Symbol	68 Lead			52 Lead			84 Lead		
	Min	Max	Notes	Min	Max	Notes	Min	Max	Notes
A	0.165	0.190		0.165	0.180		0.165	0.190	
A ₁	0.090	0.120		0.090	0.120		0.090	0.120	
D	0.985	0.995		0.785	0.795		1.185	1.195	
D ₁	0.950	0.958		0.750	0.756		1.150	1.158	
D ₂	0.890	0.930		0.690	0.730		1.090	1.130	
E	0.985	0.995		0.785	0.795		1.185	1.195	
E ₁	0.950	0.958		0.750	0.756		1.150	1.158	
E ₂	0.890	0.930		0.690	0.730		1.090	1.130	
N	68			52			84		
CP	0.000	0.004		0.000	0.004		0.000	0.004	
TCP	0.000	0.004		0.000	0.004		0.000	0.004	
LT	0.008	0.014		0.009	0.015		0.008	0.014	
ISSUE	IWS 10/12/88								

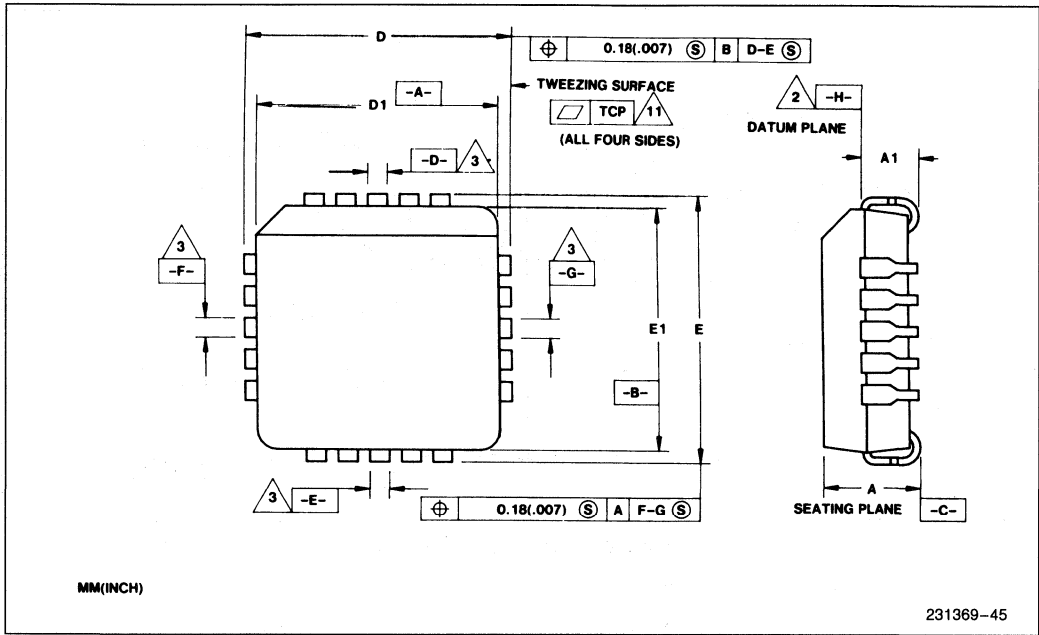


Figure 1. Principal Dimensions and Datums

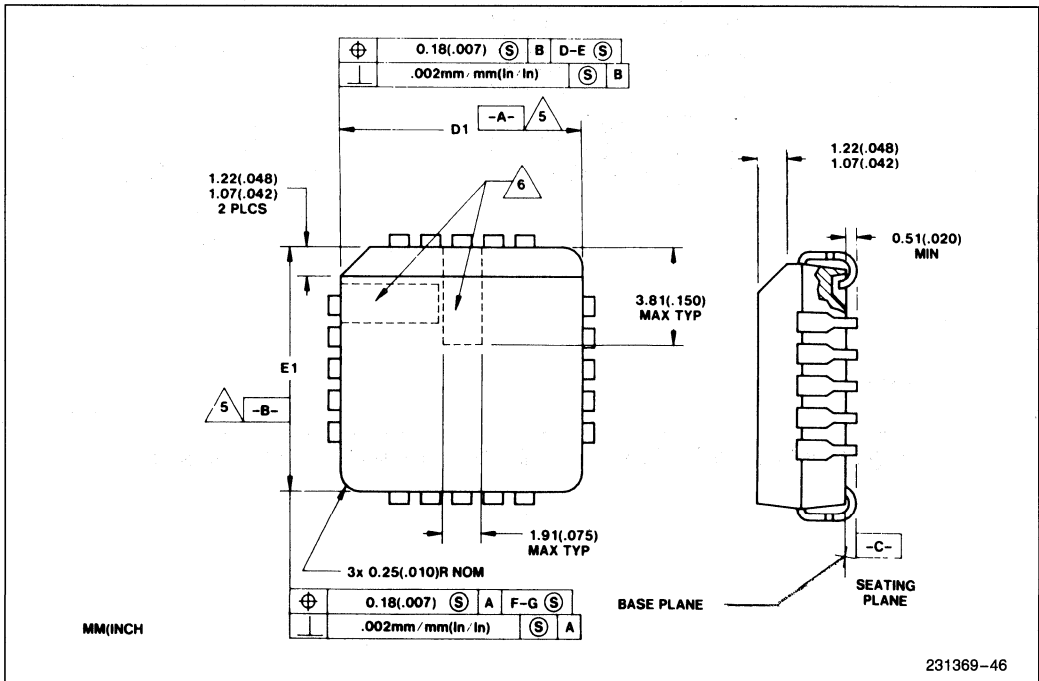


Figure 2. Molded Details

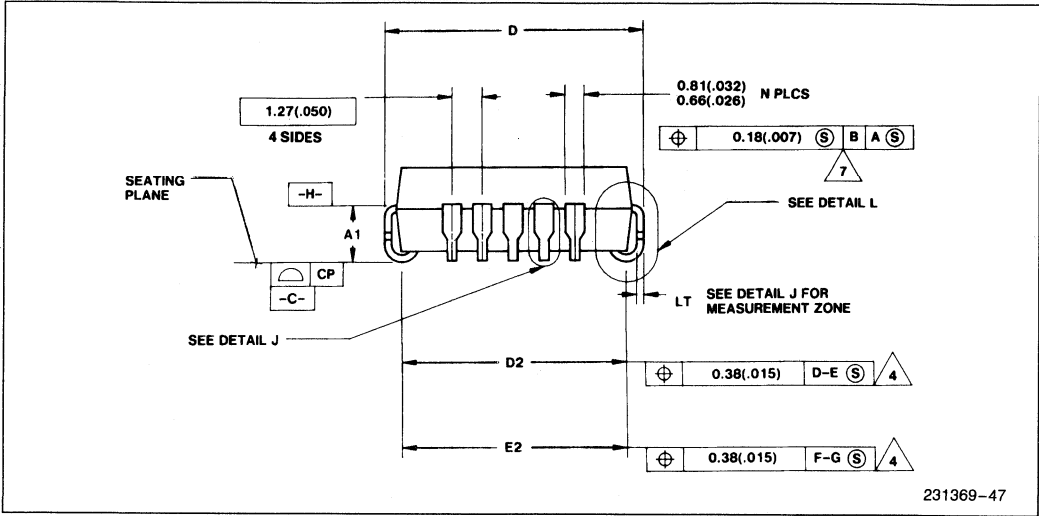


Figure 3. Terminal Details

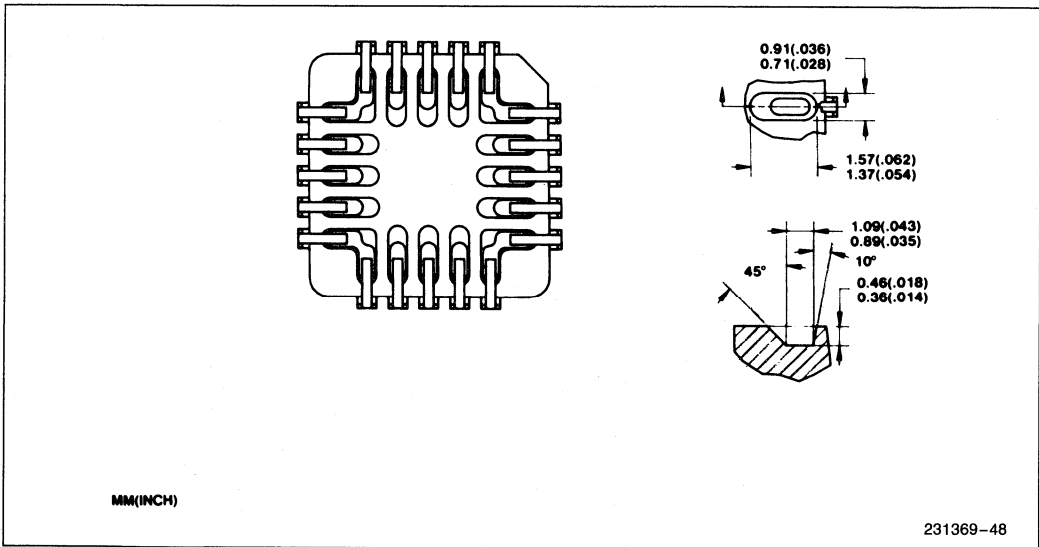


Figure 4A. Standard Package Bottom View (Tooling Option I.)

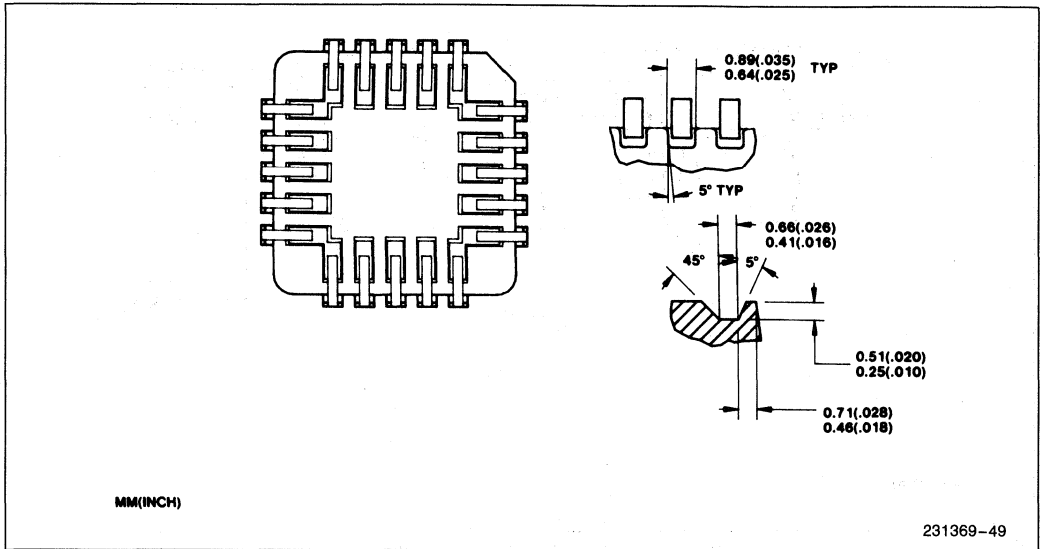


Figure 4B. Standard Package Bottom View (Tooling Option II.)

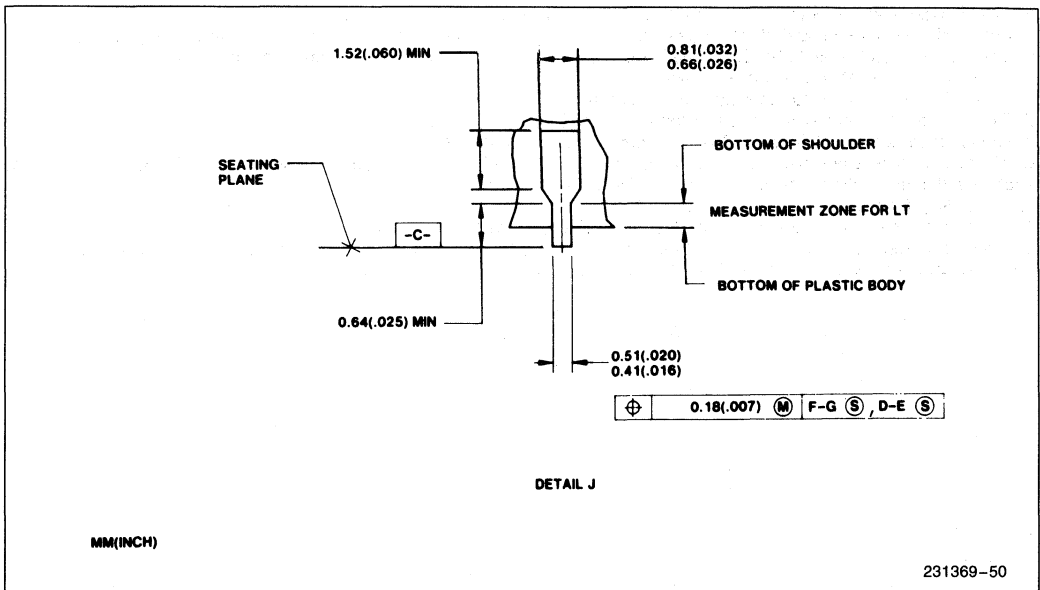


Figure 5. Detail J. Terminal Detail

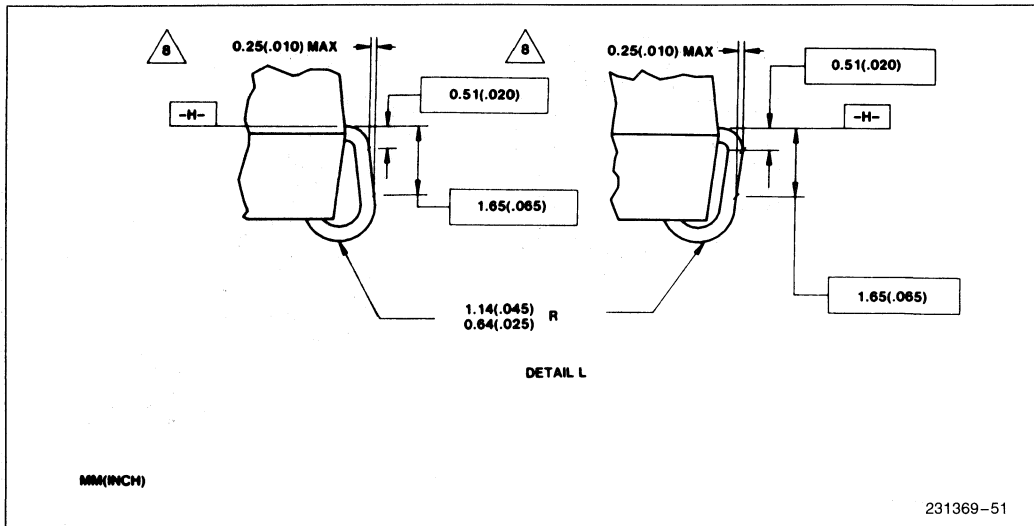


Figure 6. Detail L. Terminal Details

NOTES SQUARE PACKAGE:

1. All dimensions and tolerances conform to ANS¹ Y14.5M-1982.
2. Datum plane **H** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Datums **D-E** and **F-G** to be determined where center leads exit plastic body at datum plane **H**.
4. To be determined at seating plane **C**.
5. Dimensions D1 and E1 do not include mold protrusion.
6. Pin 1 identifier is located within one of the two defined zones.
7. Locations to datum **A** and **B** to be determined at plane **H**.
8. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
9. Controlling dimension, inch.
10. All dimensions and tolerances include lead trim offset and lead plating finish.
11. Tweezing surface planarity is defined as the furthest any lead on a side may be from the datum. The datum is established by touching the outermost lead on that side and parallel to **D-E** or **F-G**.



PLASTIC QUAD FLATPACK PACKAGE

Symbol List for Plastic Quad Flatpack Family

Symbol	Description
N	Leadcount
A	Package Height
A1	Standoff
D, E	Terminal Dimension
D1, E1	Package Body
D2, E2	Bumper Distance
D3, E3	Foot Print
D4, E4	Foot Radius Location
L1	Foot Length

2

NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane -H- located at the mold parting line and coincident with the bottom of the lead where lead exits plastic body.
3. Datums A-B and -D- to be determined where center leads exit plastic body at datum plane -H-.
4. Controlling Dimension, Inch.
5. Dimensions D1, D2, E1 and E2 are measured at the mold parting line. D1 and E1 do not include an allowable mold protrusion of 0.25 mm (0.010 in) per side. D2 and E2 do not include a total allowable mold protrusion of 0.25 mm (0.010 in) at maximum package size.
6. Pin 1 identifier is located within one of the two zones indicated.
7. Measured at datum plane -H-.
8. Measured at seating plane datum -C-.

Packaging Family Attributes	
Category	Plastic Quad Flatpack
Acronym	PQFP
Lead Configuration	Gull-Wing
Lead Counts	68, 84, 100, 132, 164, 196
Lead Finish	SolderPlate
Lead Pitch	0.025"
Board Assembly Type	Surface Mount
Standard Registration	JEDEC



PACKAGE/MODULE OUTLINES AND DIMENSIONS

Plastic Quad Flatpack (PQFP) 0.025 Inch (0.635mm) Pitch													
Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180
A1	Standoff	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
D, E	Terminal Dimension	0.670	0.690	0.770	0.790	0.870	0.890	1.070	1.090	1.270	1.290	1.470	1.490
D1, E1	Package Body	0.547	0.553	0.647	0.653	0.747	0.753	0.947	0.953	1.147	1.153	1.347	1.353
D2, E2	Bumper Distance	0.697	0.703	0.797	0.803	0.897	0.903	1.097	1.103	1.297	1.303	1.497	1.503
D3, E3	Lead Dimension	0.400 REF		0.500 REF		0.600 REF		0.800 REF		1.000 REF		1.200 REF	
D4, E4	Foot Radius Location	0.623	0.637	0.723	0.737	0.823	0.837	1.023	1.037	1.223	1.237	1.423	1.437
L1	Foot Length	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
Issue	IWS Preliminary 12/12/88												INCH

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57
A1	Standoff	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02
D, E	Terminal Dimension	17.02	17.53	19.56	20.07	22.01	22.61	27.18	27.69	32.26	32.77	37.34	37.85
D1, E1	Package Body	13.89	14.05	16.43	16.59	18.97	19.13	24.05	24.21	29.13	29.29	34.21	34.37
D2, E2	Bumper Distance	17.70	17.85	20.24	20.39	22.78	22.93	27.86	28.01	32.94	33.09	38.02	38.18
D3, E3	Lead Dimension	10.16 REF		12.70 REF		15.24 REF		20.32 REF		25.40 REF		30.48 REF	
D4, E4	Foot Radius Location	15.82	16.17	18.36	18.71	20.90	21.25	25.89	26.33	31.06	31.41	36.14	36.49
L1	Foot Length	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
Issue	IWS 4/01/90												mm

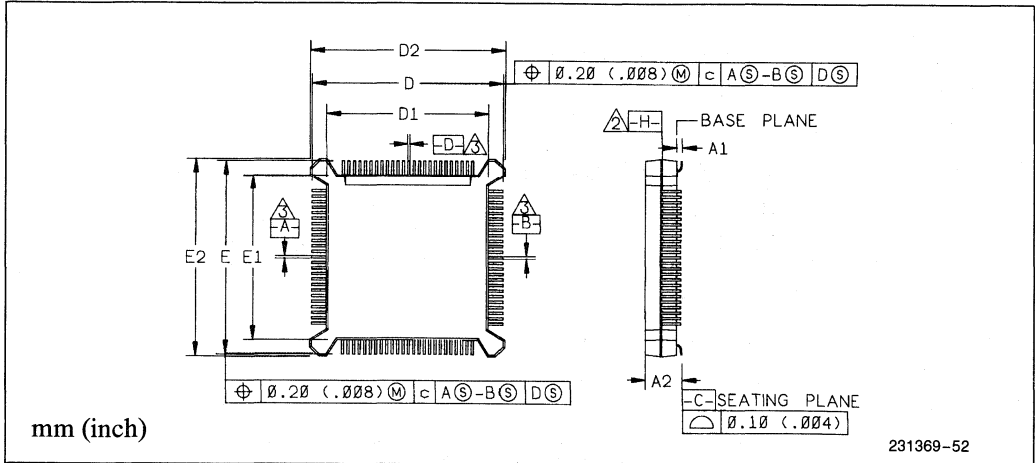


Figure 1. Principal Dimensions and Datums

2

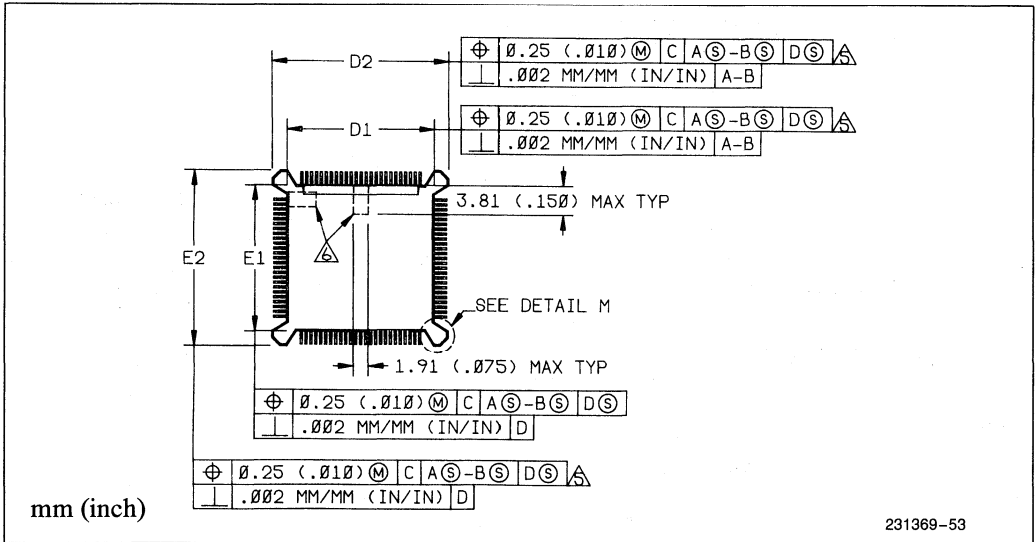


Figure 2. Molded Details

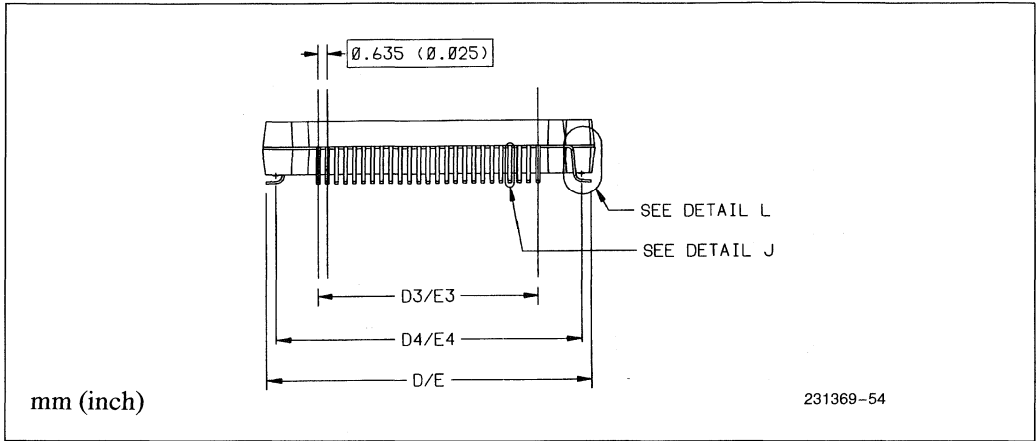


Figure 3. Terminal Details

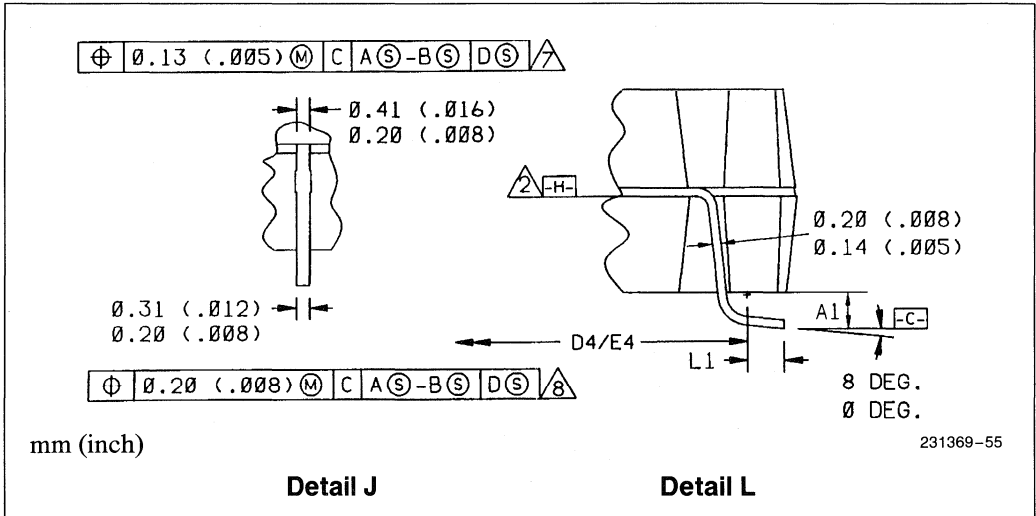


Figure 4. Typical Lead

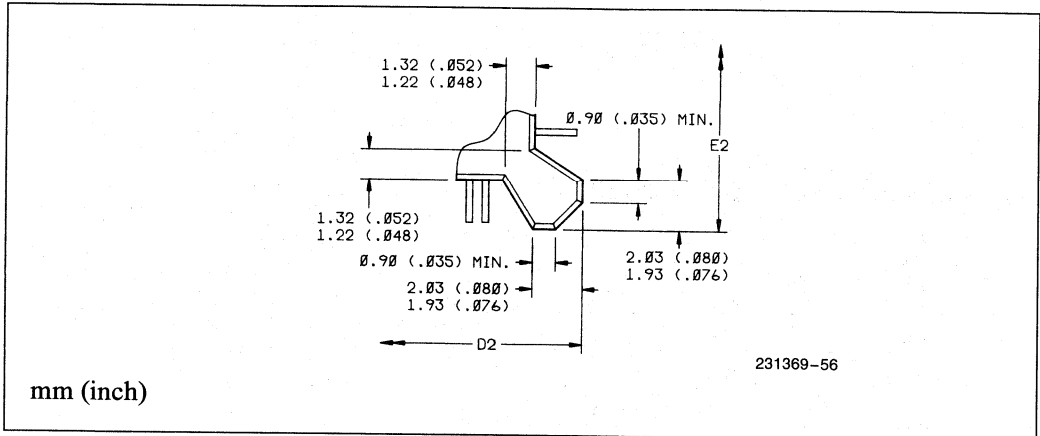


Figure 5. Detail M



QUAD FLATPACK PACKAGE

Symbol List for Quad Flatpack Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A ₁	Stand Off
B	Lead Width
C	Lead Thickness
D	Terminal
D ₁	Largest Body Dimension (Long Side)
E	Terminal
E ₁	Largest Body Dimension (Short Side)
e ₁	Lead Spacing
N	Lead Count

NOTE:

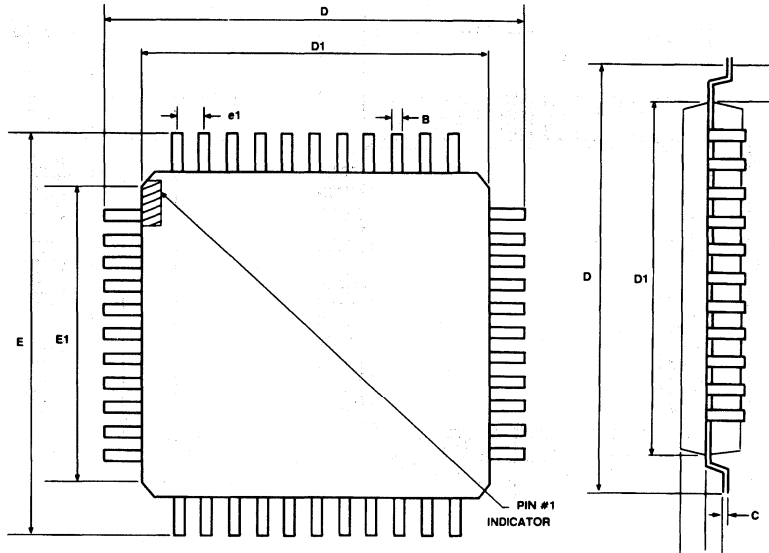
4. Not all packages are available with all products. Contact local FSE for further package information.

Packaging Family Attributes	
Category	Quad Flatpack
Acronym	QFP
Lead Configuration	Quad
Lead Counts	44, 48, 64, 80, 208
Lead Finish	SolderPlate
Lead Pitch	0.05, 0.65, 0.8 mm
Board Assembly Type	Socket and Surface Mount
Standard Registration	JEDEC and EIAJ

NOTE:

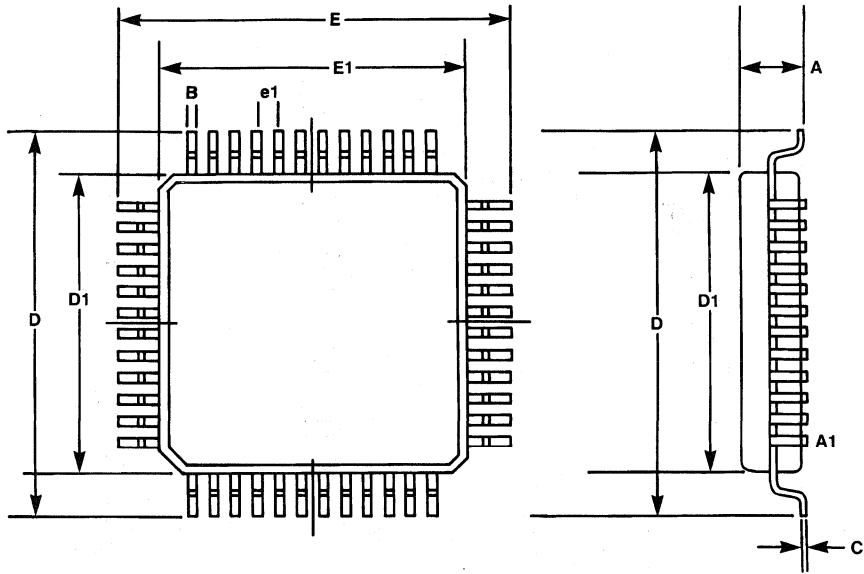
1. Alloy 42 leads.
2. Novalac body.
3. Not all packages are available with all products. Contact local FSE for further package information.

**44 LEAD QUAD FLATPACK PACKAGE
VARIATION: SQUARE**



2

Family: Quad Flatpack Package			
Symbol	Millimeters		
	Min	Max	Notes
A		2.45	
A ₁	0.0		0.10
B	.20	.45	
C	0.10	0.25	
D	11.9	12.8	12.30 Nom
D ₁	10.0		Nominal
E	11.9	12.8	
E ₁	10.0		Nominal
e ₁	.65	.95	
N	44		
ISSUE	9/19/90		

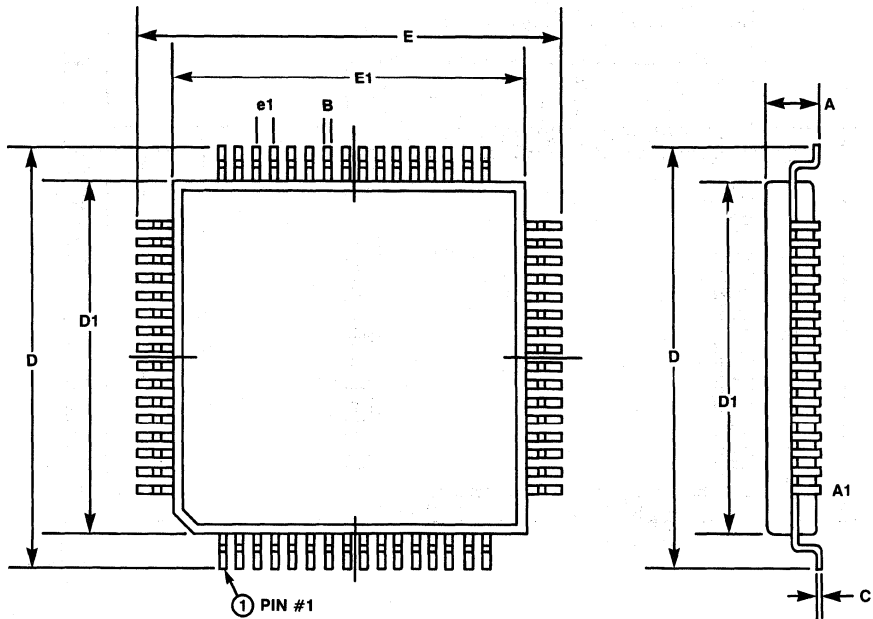
48 LEAD QUAD FLATPACK PACKAGE


231369-57

Family: Quad Flatpack Package			
Symbol	Millimeters		Notes
	Min	Max	
A		1.66	
A ₁	0.0		
B	0.14	0.26	
C	0.077	0.177	
D	8.7	9.3	
D ₁	7.0		Nominal
E	8.7	9.3	
E ₁	7.0		Nominal
e ₁	0.40	0.60	Lead Spacing
ISSUE	Preliminary		

NOTE:
Available in 1991.

64 LEAD QUAD FLATPACK PACKAGE

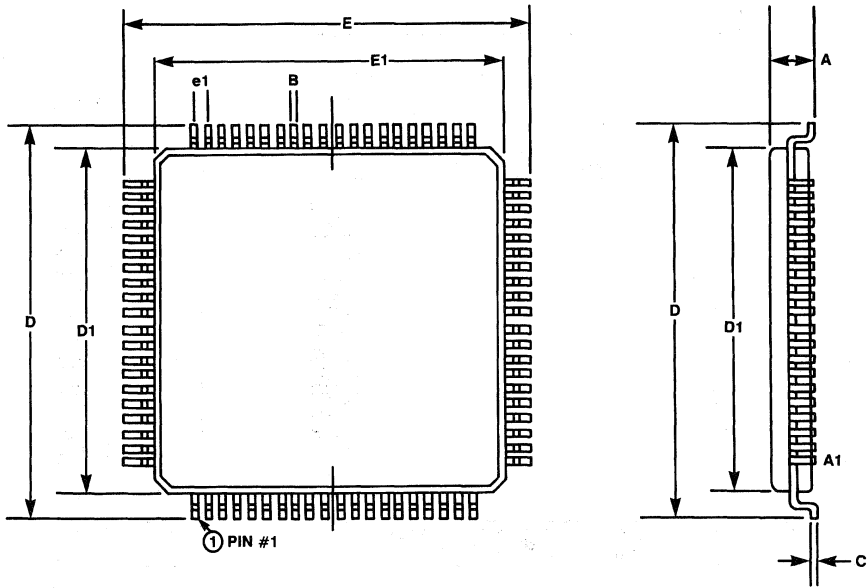


231369-58

2

Family: Quad Flatpack Package			
Symbol	Millimeters		Notes
	Min	Max	
A		2.55	
A ₁	0.0		
B	0.20	0.40	0.3 ± 0.1
C	0.05	0.25	
D	14.9	15.7	
D ₁	12.0		Nominal
E	14.9	15.7	
E ₁	12.0		Nominal
e ₁	0.53	0.77	Lead Spacing
N	64		
ISSUE			

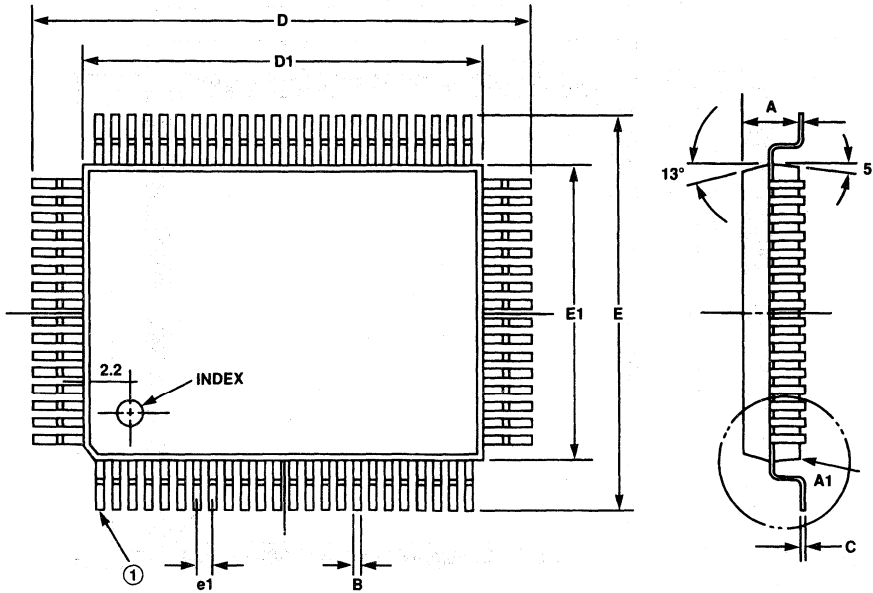
80 LEAD QUAD FLATPACK PACKAGE



231369-59

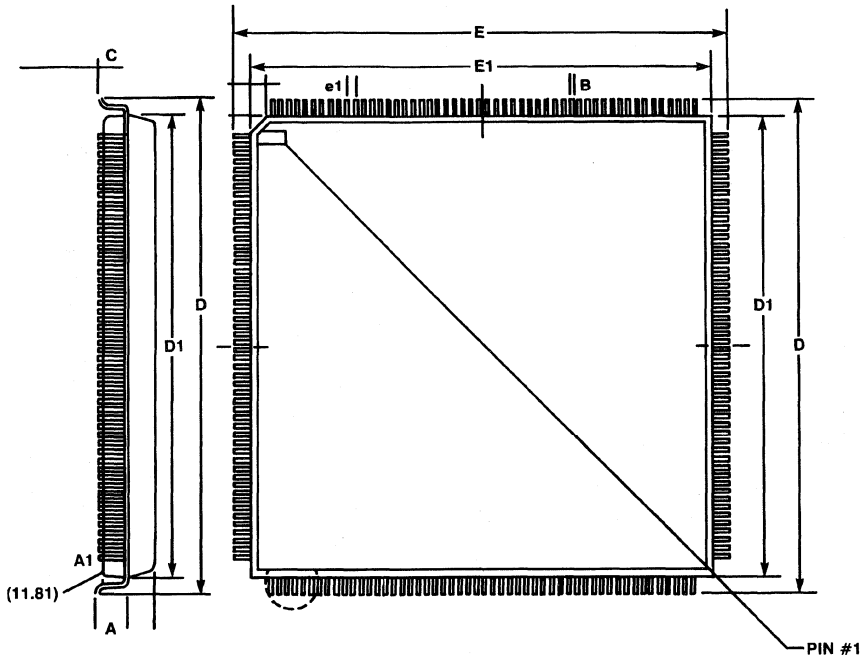
Family: Quad Flatpack Package			
Symbol	Millimeters		Notes
	Min	Max	
A		1.66	
A ₁	0.0		
B	0.14	0.26	
C	0.117	0.177	
D	13.7	14.3	
D ₁	12.0		Nominal
E	13.7	14.3	
E ₁	12.0		Nominal
e ₁	0.40	0.60	
N	80		
ISSUE	Preliminary		

**80 LEAD QUAD FLATPACK PACKAGE
VARIATION: RECTANGULAR**



2

Family: Quad Flatpack Package			
Symbol	Millimeters		
	Min	Max	Notes
A		2.9	
A ₁	0.0		
B	0.25	0.45	
C	0.1	0.2	
D	23.5	24.3	
D ₁	20.0		Nominal
E	17.5	18.3	
E ₁	14.0		Nominal
e ₁	0.65	0.95	
N	80		
ISSUE	9/19/90		

208 LEAD QUAD FLATPACK PACKAGE


231369-60

Family: Quad Flatpack Package			
Symbol	Millimeters		Notes
	Min	Max	
A		3.56	
A ₁	0.0		
B	0.10	0.30	0.25 Typical
C	0.10	0.20	
D	29.5	30.5	
D ₁	28.0		Nominal
E	29.5	30.5	
E ₁	28.0		Nominal
e ₁	0.35	0.65	
N	208		
ISSUE	Preliminary		



SMALL OUT-LINE J-LEAD PACKAGE (SOJ)

Symbol List for Small Out-Line J-Lead Family

Letter or Symbol	Description of Dimensions
A	Overall Height
A ₂	Distance from Base Plane to Highest Point of Body (Lid)
B	Width of Terminal Leads
B ₁	Width of Terminal Lead Shoulder Which Locate Seating Plane (Standoff Geometry Optional)
D	Largest Overall Package Dimension of Length
E	Largest Overall Package Width Dimension Outside of Leads
E ₁	Body Width Dimension Not Including Leads
e ₁	Linear Spacing between Center Line of Body Terminal Leads (Standoffs)
e _A	Linear Spacing of True Minimum Lead Position Center Line to Center Line
N	Total Number of Leads

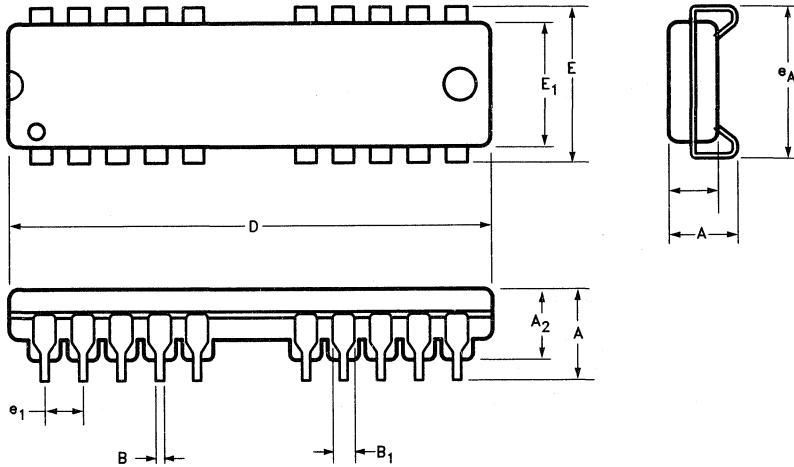
2

Packaging Family Attributes	
Category	Small Outline J-Lead
Acronym	SOJ
Lead Configuration	Dual-In-Line
Lead Counts	28
Lead Finish	SolderPlate
Lead Pitch	0.050"
Board Assembly Type	Surface Mount
Standard Registration	JEDEC and EIAJ

NOTES:

1. Alloy 42 Leads.
2. Novalac Body.

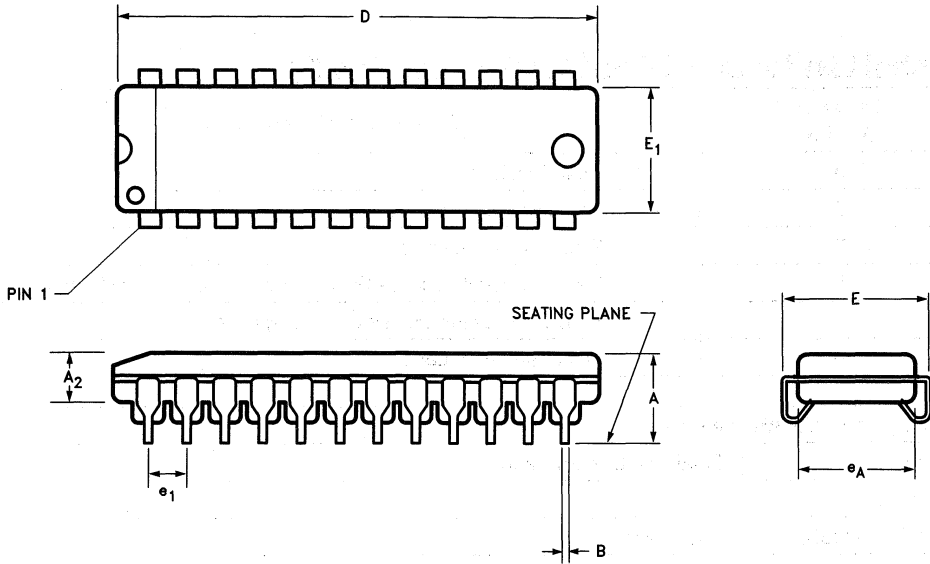
**20 LEAD SMALL OUT-LINE PACKAGE (SOJ)
VERSION: J-LEAD**



231369-61

Family: Small Out-Line J-Lead Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.04	3.61		0.120	0.142	
A ₂	2.36	3.00		0.093	0.118	
B	0.38	0.51		0.015	0.020	
B ₁	0.58	0.84		0.023	0.033	
D	17.02	17.27		0.67	0.680	
E	8.31	8.64		0.327	0.340	
E ₁	7.49	7.75		0.295	0.305	
e ₁	1.27		Typical	0.050		Typical
e _A	6.60	6.99		0.260	0.275	
e _B	7.62	10.16		0.300	0.400	
N	20			20		
ISSUE	9/19/90					

**24 LEAD SMALL OUT-LINE PACKAGE (SOJ)
VERSION: J-LEAD**



231369-62

2

Family: Small Out-Line J-Lead Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α						
A	3.35	3.61		0.132	0.142	
A ₁						
A ₂	2.74	3.00		0.108	0.118	
A ₃						
B	0.38	0.51		0.015	0.020	
D	15.75	16.18		0.620	0.637	
D ₂						
E	8.38	8.64		0.330	0.340	
E ₁	7.49	7.75		0.295	0.305	
e ₁	1.27		Typical	0.050		Typical
e _A	6.60	6.99		0.260	0.275	
e _B						
L						
N	24			24		
ISSUE						



SMALL OUT-LINE PACKAGE (SOP)

Symbol List for Small Out-Line Package Family

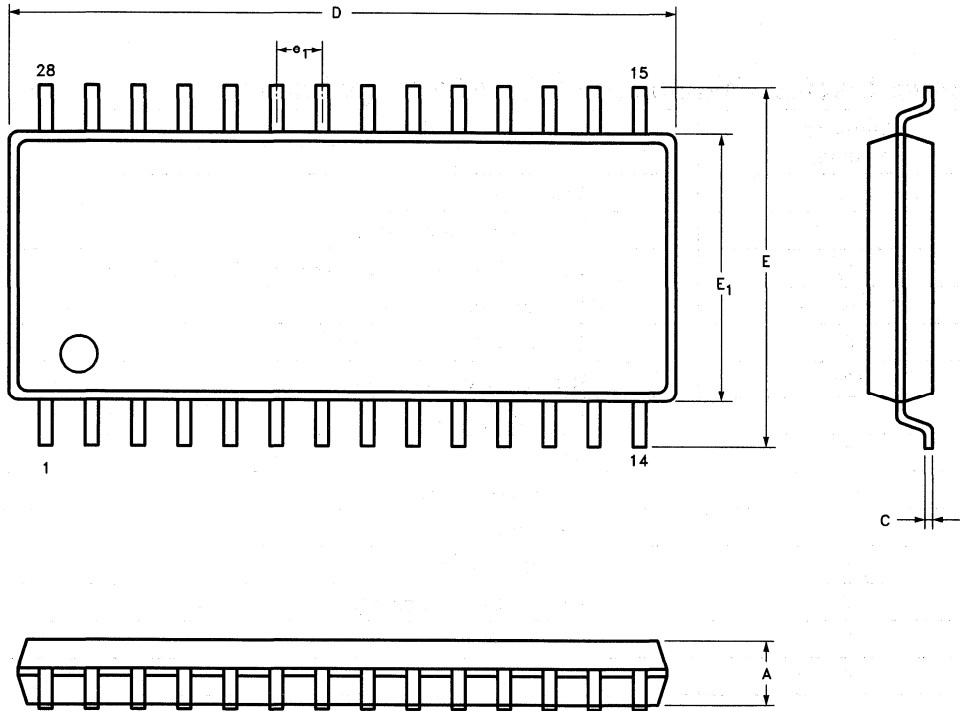
Letter or Symbol	Description of Dimensions
A	Overall Height
C	Thickness of Terminal Leads
D	Plastic Body Dimension
E	Largest Overall Package Width Dimension Outside of Leads
e ₁	Body Width Dimension Not Including Leads
N	Total Number of Leads

Packaging Family Attributes	
Category	Small Out-Line Package
Acronym	SOP
Lead Configuration	Dual-In-Line
Lead Counts	28
Lead Finish	SolderPlate
Lead Pitch	0.050"
Board Assembly Type	Surface Mount
Standard Registration	JEDEC and EIAJ

NOTES:

1. Alloy 42 and Cu Alloy Leads.
2. Novalac Body.
3. Bake and desiccant packaging required.

**28 LEAD SMALL OUT-LINE PACKAGE (SOP)
VARIATION: GULL-WING**



2

231369-63

Family: Small Out-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.62	2.87		0.103	0.113	
C	0.152	0.203		0.006	0.008	
D	17.80	18.20				
E	11.68	11.94		0.460	0.470	
E ₁	8.509	8.255		0.325	0.335	
e ₁	1.27		Typical	0.05		Typical
N	28			28		
ISSUE	9/19/90					



THIN SMALL OUT-LINE PACKAGE (TSOP)

Symbol List for Thin Small Out-Line Package Family

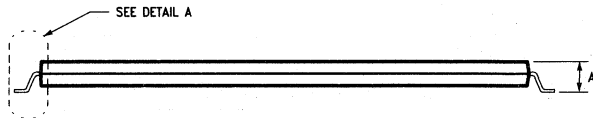
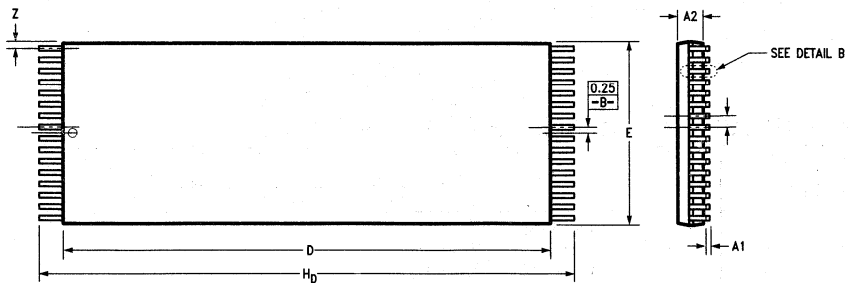
Letter or Symbol	Description of Dimensions
A	Overall Height
A ₁	Shoulder to Board Height
A ₂	Distance from Base Plane to Highest Point of Body (Lid)
B	Width of Terminal Leads
C	Thickness of Terminal Leads
CP	Seating Plane Coplanarity
D	Plastic Body Length
E	Package Body Width
H _D	Terminal Dimension
L ¹	Lead Tip Length
N	Total Number of Leads
Y	Seating Plane Coplanarity
Z	Lead to Package Offset
θ	Lead Tip Angle

Packaging Family Attributes	
Category	Thin Small Out-Line
Acronym	TSOP
Lead Configuration	Dual-In-Line
Lead Counts	32
Lead Finish	SolderPlate
Lead Pitch	0.5 mm
Board Assembly Type	Surface Mount
Standard Registration	JEDEC and EIAJ

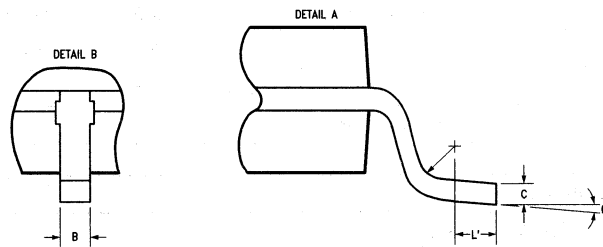
NOTES:

1. Alloy 42 Leads.
2. Novalac Body.
3. Bake and dessicant packaging required.
4. Offered in Reverse Pin-Out for special circuit layout.

32 LEAD THIN SMALL OUT-LINE PACKAGE (TSOP)



231369-64



231369-65

2

Family: Thin Small Out-Line			
Symbol	Min	Max	Notes
α	0°	5°	
A		1.20	
A ₁	0.05		
A ₂	0.96	1.06	
B	0.15	0.30	
C	0.10	0.20	
D	18.20	18.60	
E	7.80	8.20	
H _D	19.80	20.20	
L ₁	0.30	0.35	
N	32		
Y	0.00	0.10	
Z	0.20	0.30	
ISSUE	1-1-91		



PLASTIC ZIGZAG IN-LINE PACKAGE (ZIP)

Symbol List for ZigZag In-Line Package Family

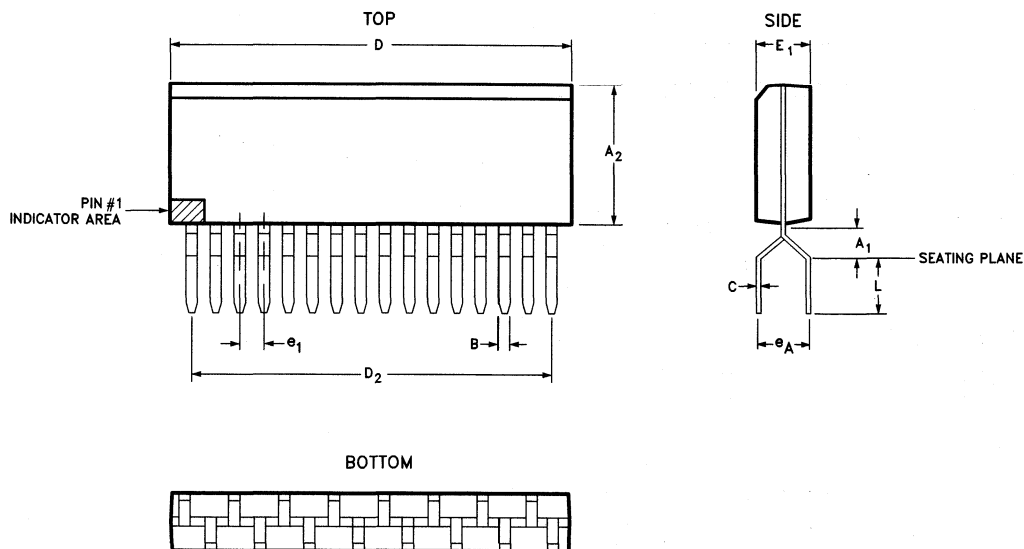
Letter or Symbol	Description of Dimensions
A	Overall Height
A ₁	Shoulder to Board Height
A ₂	Distance from Base Plane to Highest Point of Body (Lid)
B	Width of Terminal Leads
C	Thickness of Terminal Leads
D	Largest Overall Package Dimension of Length
E ₁	Body Width Dimension Not Including Leads
e ₁	Linear Spacing between Center Line of Body Terminal Leads (Standoffs)
e _A	Linear Spacing of True Minimum Lead Position Center Line to Center Line
L	Distance from Seating Plane to End of Lead
N	Total Number of Leads

Packaging Family Attributes	
Category	ZigZag In-Line
Acronym	ZIP
Lead Configuration	Dual-In-Line
Lead Counts	16, 20
Lead Finish	SolderCoat
Lead Pitch	1.27mm
Board Assembly Type	Socket or Insertion Mount
Standard Registration	EIAJ

NOTES:

1. Alloy 42 Leads.
2. Novalac Body.

16 LEAD PLASTIC ZIGZAG IN-LINE PACKAGE (ZIP)

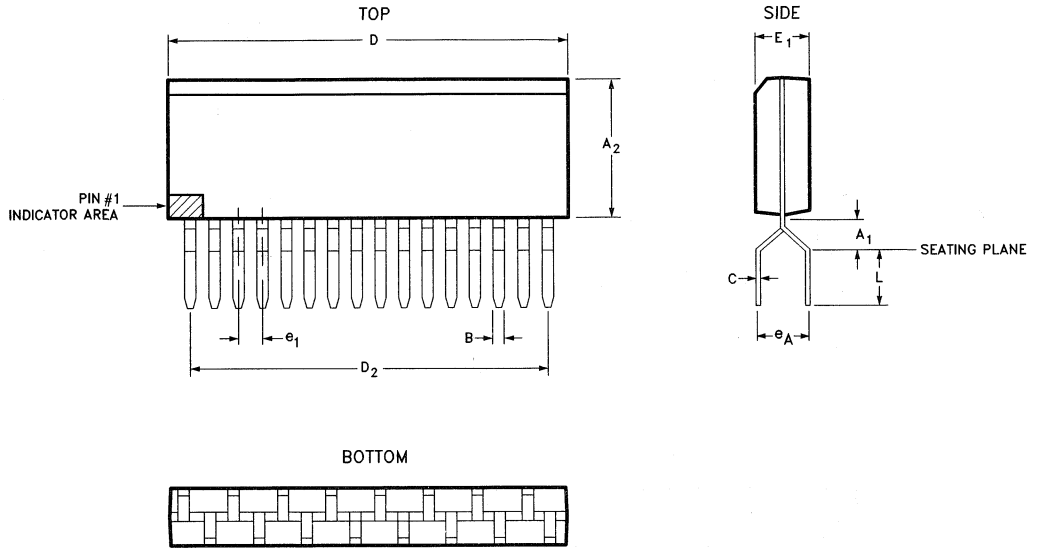


2

231369-66

Family: Plastic ZigZag In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A		8.90			0.350	
A ₁	1.14	1.91		0.045	0.075	
A ₂	6.09	6.73		0.255	0.265	
B	0.41	0.61		0.016	0.024	
C	0.20	0.36		0.008	0.014	
D	20.05	20.70		0.790	0.815	
E ₁	2.72	3.12		0.107	0.123	
e ₁	1.27		Typical	0.050		Typical
e _A	2.54		Typical	0.050		Typical
L	2.54	3.56		0.10	0.14	
N	16			16		
ISSUE						

20 LEAD PLASTIC ZIGZAG IN-LINE PACKAGE (ZIP)



231369-66

Family: Plastic ZigZag In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A		10.16			0.400	
A_2	8.26	8.51		0.325	0.335	
B	0.46	0.56		0.018	0.022	
C	0.20	0.30		0.008	0.012	
D	26.04	26.29		1.025	1.035	
E_1	2.87	3.12		0.113	0.123	
e_1		1.27	Typical		0.050	Typical
e_A		2.54	Typical		0.100	Typical
L	3.05			0.120		
N	20			20		
ISSUE						



SINGLE IN-LINE LEADED MEMORY MODULE PACKAGE (SIP)

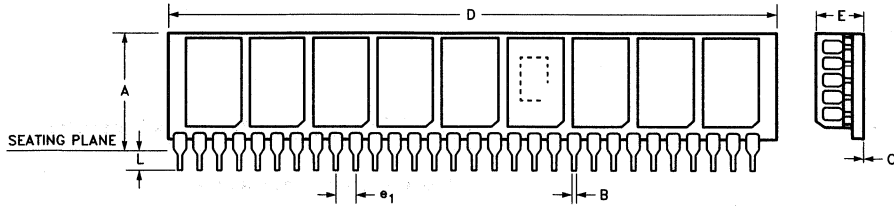
Symbol List for Single In-Line Leaded Memory Module Family

Letter or Symbol	Description of Dimensions
A	Overall Height
B	Width of Terminal Leads
C	Thickness of Terminal Leads
E	Largest Overall Package Width Dimension Outside of Leads
e_1	Linear Spacing between Centerline of Body Terminal Leads (Standoffs)
L	Distance from Seating Plane to End of Lead

2

Packaging Family Attributes	
Category	Single In-Line Leaded Package
Acronym	SIP
Lead Configuration	Single Row
Lead Counts	30
Lead Finish	Tin/Nickel
Lead Pitch	2.5 mm
Board Assembly Type	Socket and Insertion Mount
Standard Registration	JEDEC

30 LEAD SINGLE IN-LINE LEADED MEMORY MODULE PACKAGE (SIP)



231369-67

Family: Single In-Line Leaded Memory Module (SIP)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	16.43	16.59		0.647	0.653	
B	0.557	0.559		0.018	0.022	
C	0.229	0.279		0.009	0.011	
D	78.61	78.87		3.095	3.105	
E		5.08			0.200	
e ₁	2.54			0.110		
L	3.18		Typical	0.125		Typical
N	30			30		
ISSUE						



SINGLE IN-LINE LEADLESS MEMORY MODULE (SIMM)

Symbol List for Single In-Line Leadless Memory Module Family

Letter or Symbol	Description of Dimensions
B	Width of Terminal Leads
C	Thickness of Terminal Leads
D	Largest Overall Package Dimension of Length
E	Largest Overall Package Width Dimension Outside of Leads
e_1	Linear Spacing between Centerline of Body Terminal Leads (Standoffs)
N	Total Number of Leads

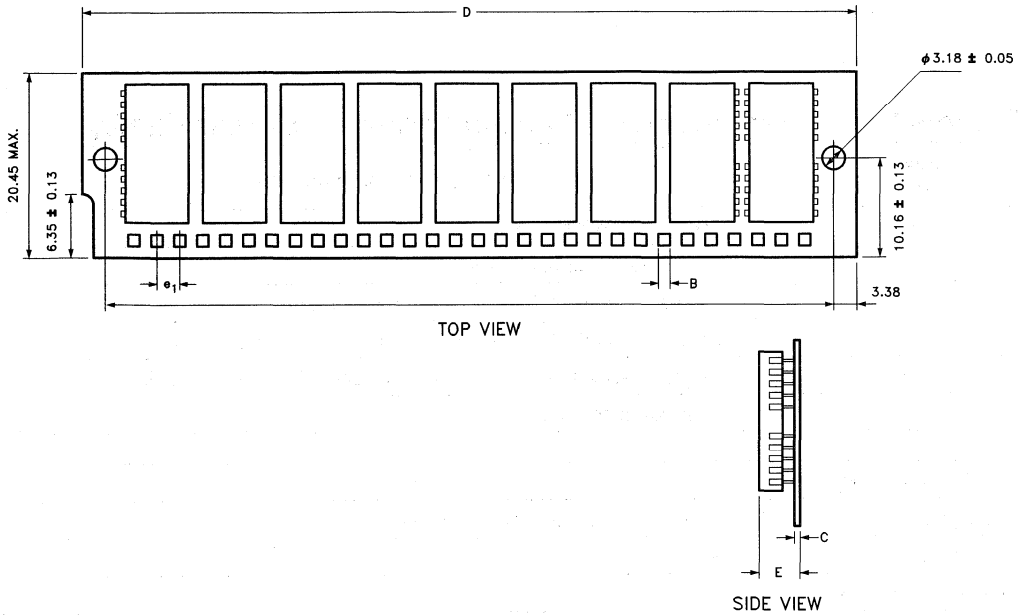
2

Packaging Family Attributes	
Category	Single In-Line Leadless Memory Module
Acronym	SIMM
Lead Configuration	Single Row
Lead Counts	30, 80
Lead Finish	SolderCoat
Lead Pitch	0.100"
Board Assembly Type	Socket and Insertion Mount
Standard Registration	JEDEC

NOTES:

1. Alloy 42.
2. Plastic body.

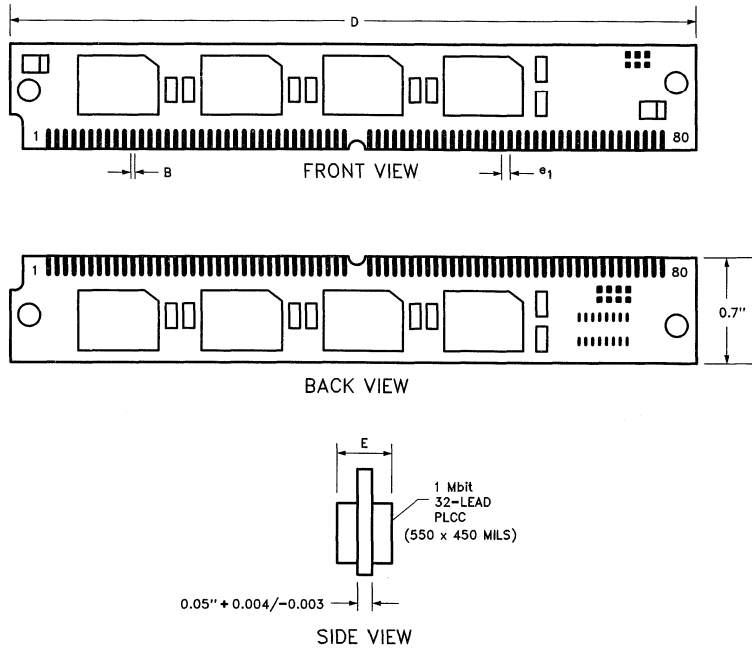
30 PIN SINGLE IN-LINE LEADLESS MEMORY MODULE (SIMM)



231369-68

Family: Single In-Line Leadless Memory Module						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
B	1.78		Typical	0.070		Typical
C	1.19	1.40		0.047	0.055	
D	88.77	89.03		3.495	3.505	
E		5.08			0.200	
e ₁	2.54		Typical	0.100		Typical
N	30			30		
ISSUE	9/19/90					

80 PIN SINGLE IN-LINE LEADLESS MEMORY MODULE (SIMM)



2

231369-69

Family: Single In-Line Leadless Memory Module						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
B	1.04		Typical	0.041		Typical
C	1.19	1.37		0.047	0.054	
D	117.98	118.24		4.645	4.655	
E	8.38			0.33		
e ₁	1.27		Typical	0.050		
N	80			80		Typical
ISSUE	IWS	9/19/90				



CHAPTER 3 IC ASSEMBLY TECHNOLOGY

INTRODUCTION

The material and process technology steps used to manufacture or assemble Intel's three basic types of component packages differ only in detail.

The package families, described in Chapter 1, provide the functional specialization and diversity required by our customers. Material and construction attributes of individual family members are provided by the following package technologies: (1) laminated ceramic, (2) pressed ceramic, and (3) molded plastic.

As shown in Table 3-1, not all combinations of package families (form, fit, function) and package assembly technologies are available.

Figure 3-1 illustrates the package assembly steps common to the three basic package technologies. The descriptions of Intel assembly technologies that follow are arranged in sequence of these process steps, and are preceded by a description of the statistical methods used throughout process development to ensure a reliable, high-quality, manufacturable product.

3

Table 3-1. Intel Package Families and Technologies

Package Family	Package/Assembly Technologies		
	Single Layer		Multilayer
	Pressed Ceramic	Molded Plastic	Laminated Ceramic
Dual In-Line Pin (DIP)	X	X	X
Chip Carrier:			
Leadless			X
Leaded	X	X	X
Pin Grid Array			X

STATISTICAL TOOLS IN ASSEMBLY TECHNOLOGY

Statistical tools are critical to achieving the high yields and extremely low defect levels required in today's competitive component manufacturing environment.

As shown in Figure 3-2, new Intel processes undergo three development phases using a wide variety of statistical tools prior to production:

- Feasibility demonstration
- Process characterization
- Manufacturing validation

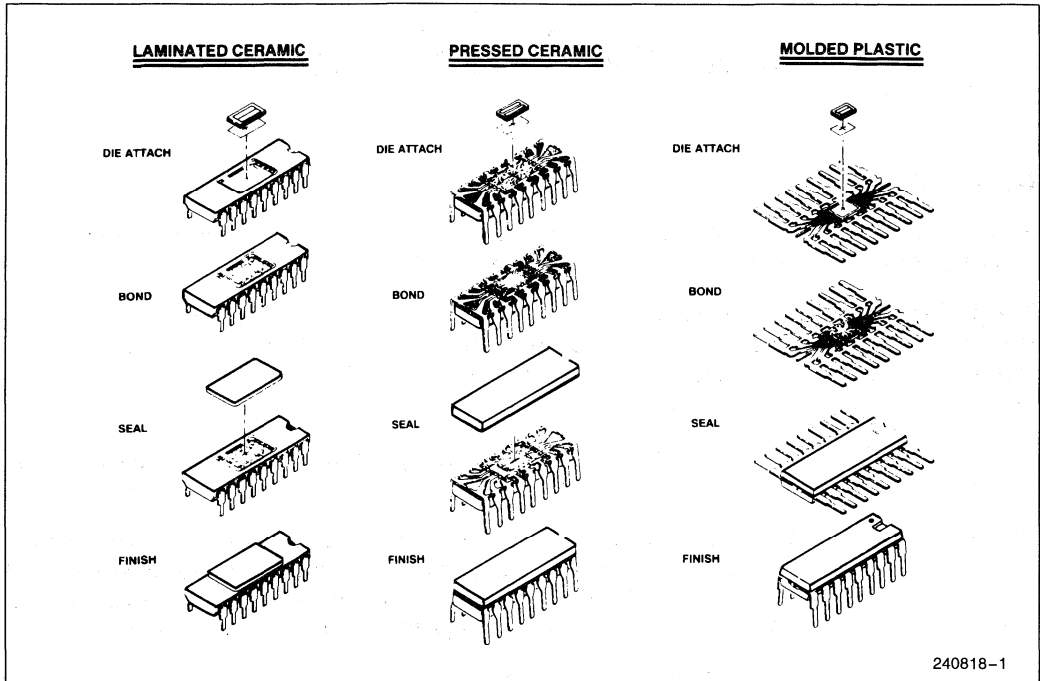


Figure 3-1. Generic Package Technologies—Process Steps

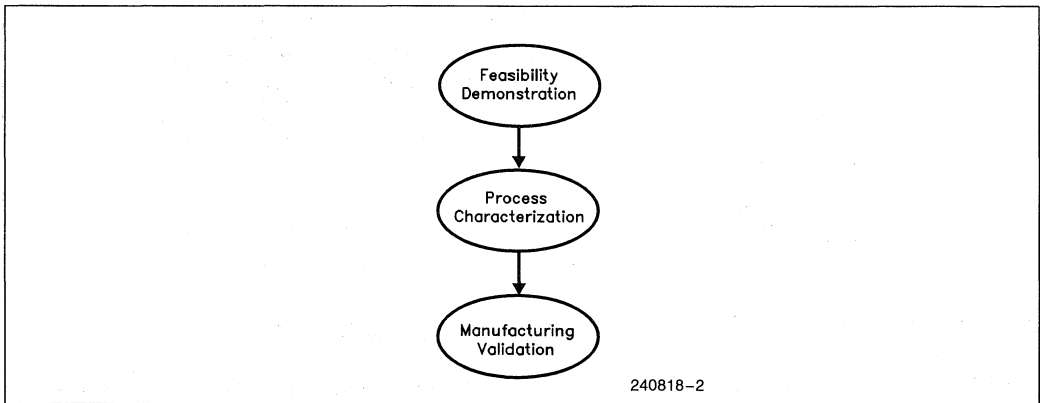


Figure 3-2. Development Statistical Methods Model

Feasibility Demonstration

At this stage of development, Intel engineers use small laboratory experiments to determine the manufacturability of a new process. Obvious design flaws and process difficulties, as well as areas in which the process differs significantly from expectations, are identified during feasibility demonstration.

The most valuable statistical tools used to determine feasibility are simple graphical techniques, including scatter plots, histograms, boxplots, and bar graphs. While data may be insufficient to represent the process variation fully, plotting of the data provides the insight necessary for making critical decisions on the process.

Process Characterization

During this phase, Intel engineers characterize process performance by determining how all important input variables to the process (e.g., temperature and material characteristics) affect the response or output variable of the process to be measured, such as bond line thickness, adhesion, package moisture content, and package reliability under environmental stress.

Process characterization makes extensive use of systematic design of experiments (DOE) methodology. In planning experiments, DOE allows consideration of all important input and output variables and includes such techniques as randomization, replication, and blocking. A common type of experiment is the factorial design, in which combinations of factors are changed systematically to learn how factors interact to affect a specific response.

In the early development phases of a new process when there is usually a wide range of variables to consider, Intel engineers study a fraction of the many combinations of variables possible, thus conserving resources. These experiments are known as fractional factorial designs or screening designs. As more is understood about a process, some variables may be set constant at optimum levels, while others continue to be investigated and refined in follow-up experiments. This “phased experimentation” approach systematically identifies and modifies variables until the critical process parameters have been determined and an optimum operating window has been established.

Often during the process characterization stage, Intel engineers must develop the metrology for a given process. In this case, a measurement capability study is a useful tool for ensuring that the measurement process can provide the precision required.

Another key statistical tool useful in the characterization phase is the process capability study. During these studies, Intel engineers use control charts such as the one shown in Figure 3-3 to monitor critical process parameters at regular intervals and examine process stability over time.

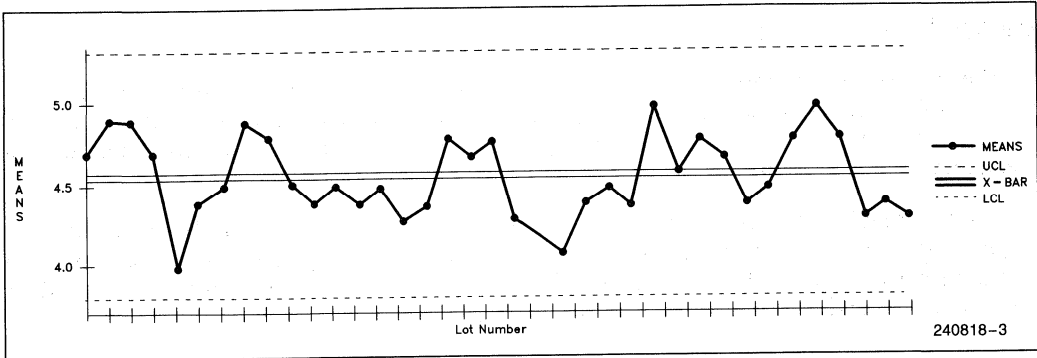


Figure 3-3. X-Bar Control Chart, Bond Line Thickness (mils)

As shown in Figure 3-4, problem-solving tools such as cause-and-effect (fishbone) diagrams and process flow charts are useful in all stages of process development and are invaluable during the design of an experiment.

Manufacturing Validation

During the manufacturing validation stage, the process is piloted in Intel's Advanced Manufacturing Module (AMM), an engineering development line where processes/products are engineered and fully characterized before introduction to assembly production lines. At this time, results of the characterization are verified using production equipment, and other necessary experiments are performed. The process remains in the validation stage until it is proven and accepted as a manufacturable, high-quality, reliable process.

DIE PREPARATION

Intel protects the surface of silicon devices from handling-induced defects by using contactless handling throughout wafer processing and die singulation, the separation of dies from the wafer.

Wafer preparation for sawing is also contactless, from wafer mounting and application of supporting tape (by balanced air-pressure technique) to the sawing operation itself. Intel uses through-wafer sawing to eliminate surface contact during die separation and follows with a high-pressure DI (deionized water) wafer wash to eliminate particulate contamination.

In addition, special care is taken to minimize surface contact in all subsequent assembly process steps.

DIE ATTACH

Intel die attach materials fall into two categories: (1) adhesives, both organic and inorganic; and (2) hard solders (gold-silicon eutectic). The choice of die attach materials depends on the specific applications and is compatible with the particular packaging technologies to ensure the highest levels of performance and reliability. Table 3-2 summarizes the die attach materials used at Intel by package type.

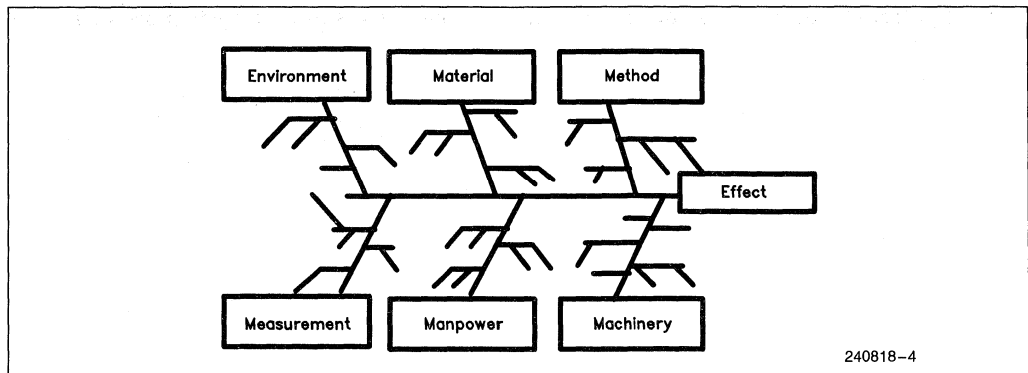


Figure 3-4. Cause/Effect Diagram

Table 3-3 is a summary of the properties of die attach materials used at Intel.

Table 3-2. Die Attach Materials by Package Type

Package	Die Attach Material	Type
Pressed Alumina Ceramic (CERDIP, Cerquad)	Silver-Filled Glass	Inorganic Adhesive
Laminated Alumina Ceramic (PGA, CQFP, Side-Braze)	Gold-Silicon Eutectic	Hard Solder
Molded Plastic (Alloy 42 Lead Frame)	Silver-Filled Polyimide	Organic Adhesive
Molded Plastic (Copper Lead Frame)	Silver-Filled Epoxy	Organic Adhesive

Table 3-3. Die Attach Material Summary

	Au-Si	Silver-Filled Glass	Silver-Filled Polyimide	Silver-Filled Epoxy
Wafer Backside Metallization for Die Attach	Required	Not Required	Not Required	Not Required
Wafer Backside Metallization for Ohmic Contact	Not Required	Required	Required	Required
Thermal Dissipation	Good	Good	Fair	Fair
Electrical Conductivity	Good	Good	Fair	Fair
Lead Frame Compatibility (a) Alloy 42 (b) Cu Alloy	N/A N/A	N/A N/A	Good Poor	Good Good
Substrate Metallization Compatibility (a) Gold (b) Silver (c) Al ₂ O ₃	Good Good N/A	Poor Good Good	Good Good N/A	Good Good N/A

Figures 3-5 through 3-7 are schematic cross-sections through each of the different die attach systems currently in use at Intel, i.e., gold/silicon eutectic, silver-filled glass, and silver-filled organic adhesives, both polyimide and epoxy. The components of each system are identified.

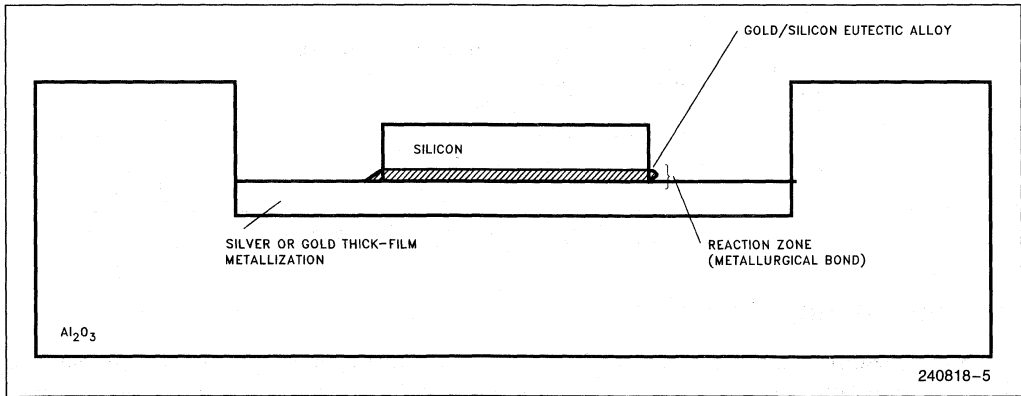


Figure 3-5. Gold-Silicon Eutectic

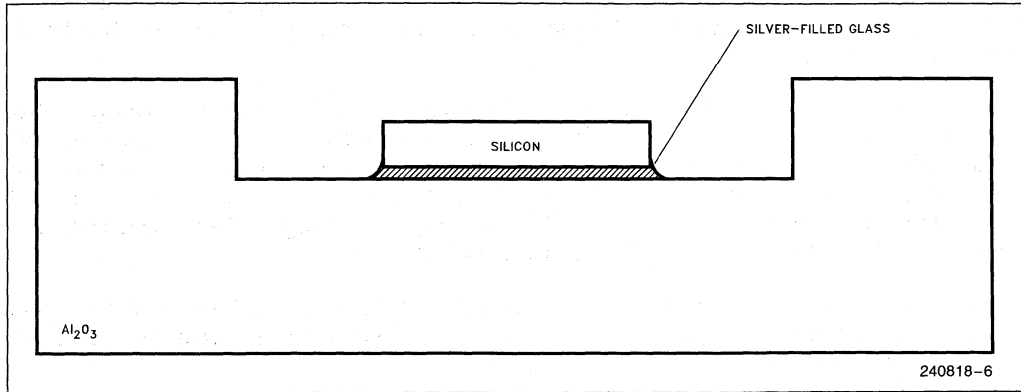


Figure 3-6. Silver-Filled Glass

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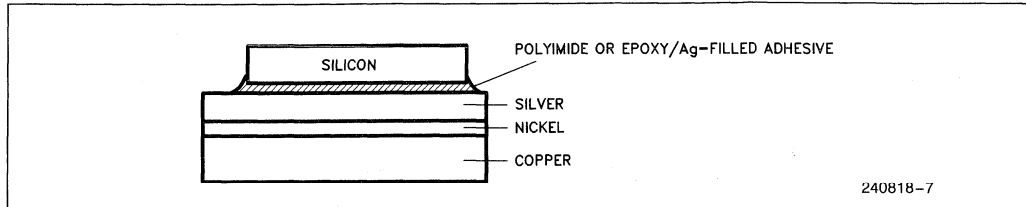


Figure 3-7. Silver-Filled Adhesive

Purpose of Each Component

The **wafer metallization** is used to provide an ohmic contact to the silicon die for the purpose of substrate biasing for those die attach media that do not readily form any ohmic junction, i.e., silver-filled glasses, epoxies, and polyimides. It provides a readily wettable surface for gold/silicon hard soldering and prevents premature oxidation (or aging) of the wafer backside during storage by acting as a diffusion barrier, thus ensuring that die attach integrity remains uncompromised.

Like the wafer backside, the **substrate metallization** is used to provide a readily wetted surface for hard soldering. The metallizations used in hermetic package technologies, both gold and silver, are readily wetted by the liquid solder at die attach temperatures and actually react with the solder to provide a high-integrity metallurgical bond to the substrate. Both substrate metallizations resist oxidation, which can impede wetting, and are electrically conductive for those devices that require electrical contact.

Plastic packages use a plated silver metallization that is wetted by and adherent to organic adhesives, and that is electrically conductive. Silver-filled glass does not require a metallization, though it will adhere quite readily to silver.

The **die attach media** themselves serve several purposes other than the obvious one of attaching the silicon to the substrate. They also provide a means of making an electrical connection to the die backside for those devices requiring it, as well as a path for conduction of heat from the die to the ambient. For these reasons, the die attach media used at Intel exhibit good thermal and electrical conductivity.

The incoming quality of die attach materials is monitored through a series of specifications unique to each of the die attach media. Tests are performed at Intel and by our material vendors to measure those specific characteristics necessary to ensure that materials meet the requirements of die attach applications.

Process Limitations

From the standpoint of process design, it is necessary to understand the limitations of each die attach process. Each of the die attach technologies used at Intel has its own limitations with an impact on applications.

Au-Si EUTECTIC

There are three key limitations to this process. Foremost is the effect of processing temperature on die reliability and performance; it is necessary to design silicon fabrication processes so that they can withstand the Au-Si process temperatures for the die attach duration. Next is the need for die backside metallization for even moderate die sizes and for those applications demanding the highest reliability. All Intel dies use a wafer backside metallization. The third limitation is the need for excellent process control. This limitation is discussed in a later section.

SILVER-FILLED GLASS (SFG)

SFG, like Au-Si eutectic, is limited to those devices that can withstand the SFG processing temperature and time. Again, the silicon fabrication processes need to be designed to withstand the die attach process. Because of the organic content (solvent and resin binder) of the SFG paste, there are limits on the minimum dry times versus die size that constrain the process. Larger dies mean longer drying/processing times.

There are also limits to the bond line thickness, both thin and thick, that constrain the process. In addition, it is imperative to maintain a nearly void-free die attachment. SFG is limited to (1) nongold wafer backsides and substrates due to poor adherence to gold, and (2) inert or oxidizing processing ambients.

Like Au-Si eutectic, SFG requires close process control. Once processed, the SFG material is stable to extremely high temperatures.

SILVER-FILLED POLYIMIDE

Like SFG, the silver-filled polyimides contain a significant volume of solvent that must be carefully removed during processing to minimize voiding. Also, water vapor is released during the imidization reaction and must be carefully removed to prevent voiding.

Because of these considerations, the polyimide process must be designed properly, allowing long processing times for large dies. As die size increases, processing times may become prohibitive from a manufacturing point of view. Because of the large volume changes (shrinkage) associated with the solvent loss, die attach stress occurs; in most applications, however, this is not a concern, since the stresses tend to be compressive. However, with copper lead frames, the stress can increase to a point where the frames are damaged during processing, especially with larger dies. There is a minimum bond line thickness limitation for polyimide, below which stresses on the die can increase.

Polyimide adhesives are stable to very high temperatures and are not affected by temperature exposure during subsequent processing. The polyimide material used at Intel is stable to at least 450°C for short periods of time.

SILVER-FILLED EPOXY

There are two significant limitations on epoxy. The first is the upper temperature that the material can tolerate before decomposition occurs, which is approximately 200°C. The second is a limitation on the minimum bond line thickness, again a die stress concern. As with the other paste technologies, it is important to maintain a nearly void-free die attachment through control of the dispensed paste volume.

Processes

Au-Si

Figure 3-8 is a representation of the gold-silicon phase diagram. In this process, a pure gold preform is placed into a preheated ceramic package under a heated inert gas. The die is placed onto the preform and allowed to reach the preset die attach temperature.

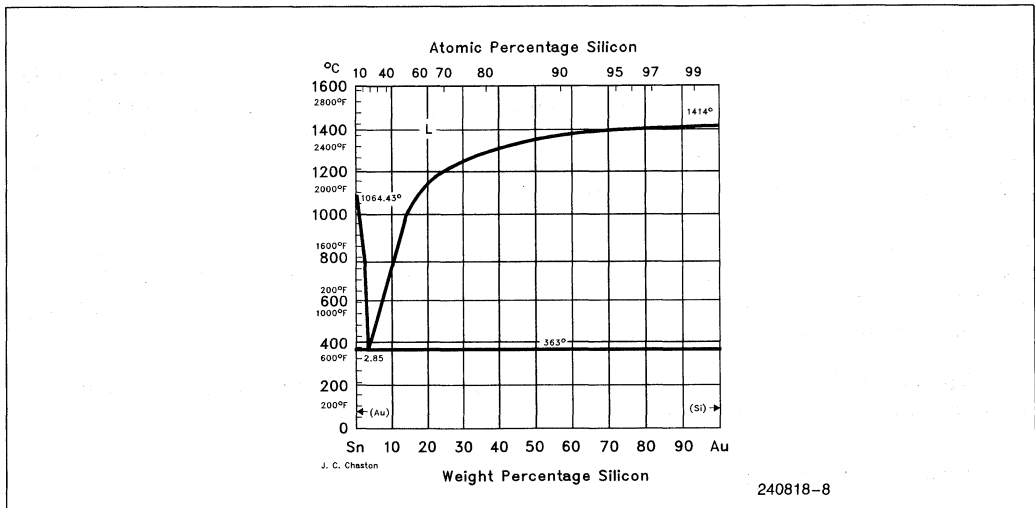


Figure 3-8. Au-Si Gold-Silicon

As the temperature is raised, silicon from the die begins to diffuse through the diffusion barrier on the die backside, and at 363°C, forms eutectic composition liquid. Once liquid formation occurs, the reactions proceed rapidly by liquid phase diffusion. As the temperature increases beyond the eutectic temperature, more silicon is dissolved from the die backside until the equilibrium volume of silicon is reached. The liquid also begins to dissolve the gold or silver substrate. The amount of gold or silver that dissolves depends on the temperature and the time of die attach.

At this point, a circular motion is used to distribute the liquid evenly across the silicon backside to ensure intimate contact with all areas. Once this is accomplished, the package and die are cooled. During cooling, silicon begins to precipitate from the saturated gold-silicon liquid. These precipitates grow epitaxially from the silicon die backside. Analysis using a transmission electron microscope has confirmed that the epitaxial region is continuous with

the bulk silicon crystal structure. When the package again reaches the eutectic temperature, the solder solidifies with a characteristic eutectic-type microstructure. There is no solid solubility of silicon in gold or vice versa, as evidenced by the phase diagram for the system. The joint obtained upon cooling is metallurgically continuous from the substrate to the die.

SILVER-FILLED GLASS

Silver-filled glass is a suspension of silver and low-softening temperature glass particles in an organic vehicle. In this process, the paste is automatically applied to the ceramic via a paste dispense system. After the paste is applied, the die is positioned within the dispensed pattern. Because of the high organic content of the paste, the SFG is carefully dried in a continuous furnace to remove the solvent. This leaves behind a resin that binds the silver and glass particles until subsequent processing can soften the glass. After drying, the material is carefully heated to remove the binder; the heating rate is determined by die size.

At higher temperatures, the glass begins to soften, and the silver particles begin to sinter together into a cohesive mass. Considerable shrinkage accompanies the reactions at higher temperatures, and care must be taken to ensure that the minimum bond line thickness requirements are maintained after shrinkage. At the highest temperatures, the glass wets the silver particles, silicon surface, and ceramic substrate, creating a strong chemical bond between the silicon and the ceramic. Once the material has reached the maximum density, the package is cooled and readied for subsequent assembly operations.

3

SILVER-FILLED POLYIMIDE

The processing for silver-filled polyimide, because it is a solvent-filled system, is similar to that of silver-filled glass. The paste is dispensed and the die positioned on automatic equipment similar to that used for SFG. Once again, it is necessary to remove the solvent from the system in a drying step prior to the imidization reaction. The drying operation is again dependent on die size (diffusion length) and has been designed to be compatible with all die sizes.

After drying, the polyimide is raised in temperature to initiate the imidization reaction. This reaction generates water vapor, and thus care must be exercised to ensure that the water is fully removed during the process. Like drying, this operation depends on die size and has been carefully designed to maximize water vapor desorption.

At the highest processing temperatures, the polyimide fully cures and forms a strong chemical bond to the lead frame and silicon. At this point, the package is cooled and sent to the subsequent assembly operation.

SILVER-FILLED EPOXY

The silver-filled epoxy used by Intel is a so-called solventless system, which eliminates the processing issues associated with drying. Because of the chemical structure of epoxy, water vapor evolution during process is also not a concern. As with the other paste technologies (polyimide and SFG), the paste is automatically dispensed and the die positioned on automated equipment, with care taken to ensure a void-free die attach. After placement, the package is heated to the epoxy resin cure temperature to polymerize the epoxy and create the final chemical bond between the silicon and lead frame.

BACKSIDE REQUIREMENTS AND CONTROLS

The wafer backside process can have an effect on the integrity of the joint created during die attach. From gold-silicon eutectic work, Intel has determined that a metallized surface is required for highly reliable joining. The quality of the metallization modulates the wetting of the liquid to the silicon and enhances the quality of the braze joint. It has also been determined that the roughness of the surface plays a significant role in eutectic die attach, and that smooth surfaces wet more readily and more quickly than rougher ones.

Because there is a need to prevent premature oxidation of the metallization, a diffusion barrier is necessary. The barrier is required to adhere to both silicon and gold, yet not interfere with the integrity of the final joint. Finally, the barrier kinetics also must allow rapid diffusion of silicon at the die attach temperatures. Because of this, it is necessary to control the thicknesses of the barrier metal. The gold thickness must also be controlled to prevent oxidation of the barrier metal.

OHMIC CONTACT

Some MOS devices require an ohmic contact to the die backside. To achieve an ohmic contact, a metallization is required for all of the paste technologies, as the silver will not form a low-resistance ohmic contact at any of the die attach times or temperatures. An ohmic contact can be achieved with gold-silicon eutectic die attach without the use of a metallization, as the gold readily diffuses at the die attach temperature, creating a low-resistance contact. However, in Intel's experience, a wafer backside metallization is necessary for the creation of a highly reliable eutectic joint.

Performance and Engineering Characteristics

DIE SIZE LIMITATIONS

- **Au-Si.** At this time, there are no known limits to the die size that can be attached with this technique. Dies as large as 1.8 x 1.8 cm (0.7 x 0.7 in.) have been successfully attached by this technique.
- **Silver-Filled Glass.** It has been demonstrated that dies as large as 1.0 x 1.0 cm (0.4 x 0.4 in.) can be successfully attached by this technique.
- **Silver-Filled Polyimide.** It has been demonstrated that dies as large as 1.0 x 1.0 cm (0.4 x 0.4 in.) can be successfully attached by this technique.
- **Silver-Filled Epoxy.** Because there are no limitations on solvent or water vapor evolution for this type of paste, there are no known die size limitations. Dies as large as 1.3 x 1.3 cm (0.5 x 0.5 in.) have been successfully attached using this die attach material.

JOINT STRENGTHS

Table 3-4 summarizes the die attach joint strengths and typical failure modes for each of the die attach materials used at Intel today. As shown, measured strengths easily exceed the military specifications for die attach strength as determined by tensile testing.

A typical failure mode for Au-Si is fracture of the silicon. For the other technologies, failure of the adhesive material, i.e., a cohesive failure, is typical.

Table 3-4. Typical Tensile Bond Strengths of Various Die Attach Media

Die Attach Media	Tensile Strength (kg/cm ²)	Tensile Strength (psi)
Au-Si	500	>7000
Silver-Filled Glass	140	2000
Silver-Filled Polyimide	140	2000
Silver-Filled Epoxy	140	2000

MODELING RESULTS

Modeling conducted at Intel has shown that die cracking during temperature cycling can be caused by stress risers in the die attachment. While small voids in the die attachment act as stress risers, they do not create the type of tensile forces necessary to fracture silicon. Only when voids occur at die corners or edges do tensile stresses result that can cause the silicon to fail. Typically, edge voids in Au-Si are the result of improper wetting of the liquid to the silicon surface, which causes the liquid to take up a lower surface energy configuration, and pulling away from the die edge. Subsequent temperature cycling creates a tensile stress at the void/solder interface that fractures the silicon. Proper metallization techniques minimize this risk by preventing dewetting during die attach.



The same effects can occur with the paste technologies during die attach. Therefore, it is imperative to maintain a void-free die attach, particularly edge voids. Care is taken during paste dispense to ensure that the entire die area is fully covered by die attach media to minimize the risk of edge void formation.

BACKSIDE METALLIZATION CONTROLS

Control of the wafer backside metallization process is essential for high-integrity gold-silicon eutectic bonds. As mentioned, it is important to control the thicknesses of both the barrier metal and the gold. It is also necessary to control the deposition conditions to minimize the oxygen content of the barrier metal. Failure to do so can result in a poorly wettable surface that does not allow rapid, uniform silicon diffusion at the Au-Si die attach temperatures.

WIRE BONDING

Wire bonding is an assembly step that connects the input/output of the device to the package terminals. At this stage in the assembly process, the majority of the final cost is already in the device. Thus, it is critical that the highest yield of wire bonding is achieved.

To ensure a high-quality, reliable wire bond, Intel engineers have made significant advances in techniques to control and monitor the bonding process.

Wire-Bonding Techniques

Intel wire-bonding techniques include (1) thermosonic, or gold ball, bonding; and (2) ultrasonic, or aluminum wedge, bonding.

In thermosonic bonding, a gold ball is formed at the end of the wire, and a bond is made between the bond pad surface and gold ball. With the ultrasonic bonding technique, a bond is made directly between the wire and the bond pad.

Bonding Parameters

Key bonding parameters include machine, material, and structural parameters. To achieve a high-quality wire bond, bonding parameters must be well understood and controlled.

The most important **machine parameters** are force, ultrasonic energy, temperature, and time. Controlling the interaction of these parameters is critical to bond quality and reliability.

Force is applied to establish and maintain an intimate contact between wire and metal surfaces during application of ultrasonic energy.

Ultrasonic energy is used to reduce the level of applied stresses necessary for plastic deformation of wire and metal surfaces by generating a larger number of mobile dislocations.

Heat (thermal energy) is applied in thermosonic bonding to compensate for ultrasonic energy attenuation by gold ball and ultrasonic reflection at the interface of ball and bond pad metallization. Applied thermal energy helps to reduce the level of stresses necessary for plastic deformation of substrate metallization.

Finally, the function of the parameter time is to control the amount of plastic deformation at the gold ball/pad metallization interface for bonding.

A number of **material and structural parameters** also have significant impact on the quality and reliability of the wire-bonding process and are strictly controlled. Intel works closely with wafer fab process development teams and our wire and lead frame vendors to obtain required characteristics for wire, metal surfaces, and structural parameters.

Critical parameters for wires are diameter, tensile strength, elongation, composition, and surface contamination.

For metal surfaces, controlled parameters include surface hardness, roughness, cleanliness (freedom from glass residues, oxide, silicon dust), and structural parameters.

Key structural parameters include (1) shape and dimensions of bonding surfaces (bond pad and lead tip); (2) number, thickness, and mechanical properties of underlayer materials; (3) integrity of underlayer interface (adhesion of underlayer materials); and (4) material interactions among wire-bonding elements, such as interdiffusion and intermetallic compound formation.

Bonding Process Quality Tools

To achieve high-quality wire bonds, Intel precisely measures and optimizes all bonding parameters. A number of techniques and bonding process quality tools have been developed for measuring the parameters of force, ultrasonic energy, time, and temperature, and have contributed significantly to improved bond quality and reliability.

FORCE MEASUREMENT

It is essential to measure the actual force applied to wire and metal surfaces—the work piece—during bonding. The applied force usually consists of two distinct elements: dynamic and static components. To measure the actual force applied to the work piece during the bonding cycle, Intel uses a dynamic force measurement system (DFM). The heart of the system is a very fast-response transducer with extremely high sensitivity to small force changes of ± 1 gram. The DFM system allows Intel to measure the actual applied force in real time. With this technique, we can identify the following:

- Actual bond force duration and amplitude
- Dynamic and static force portions of the force curve
- Repeatability of applied force from one bond to another
- Machine-related problems affecting the force curve
- Timing for the application of ultrasonic energy as compared to the force curve
- Methods for duplicating the optimized force from one machine to another

Another important bonding parameter is time, which controls the level of plastic deformation in wire and substrate metallization. During the selected time, ultrasonic energy and force are applied to the wire and substrate. The application of ultrasonic energy to the work piece at the desired time, during the application of force, is called the timing factor. This parameter ensures consistent bond quality and reliability. The timing factor can be adjusted using the DFM unit.

ULTRASONIC MEASUREMENTS

To obtain optimum wire-bonding results, Intel continually measures the amount of ultrasonic energy applied to the wire or substrate.

A laser interferometry system and a special tool that precisely gauges the amount of displacement of the bonding tool tip are used for these measurements. As a result, we can perform the following with a high degree of accuracy:

- Measure the amount of ultrasonic energy
- Duplicate the optimum values on other bonders
- Inspect the machine set-up
- Inspect all incoming transducers for efficiency
- Detect defective transducers or inadequate mechanical coupling

TEMPERATURE MEASUREMENTS

Another major bonding parameter is thermal energy, which is applied to the substrate. An incorrect bonding temperature can result in a number of bonding problems. For example, high temperature can result in softer bond pad metallization, which causes metal splash and bond pad fracture. A temperature that is too low can result in harder metallization and consequently prevent materials from sticking.

Using an infrared monitor system instead of thermocouple, Intel can measure the exact temperature of bonding surfaces. We can also identify any design or material-related problems in our heater block system. As a result, we have achieved superior control of our bonding process.

Bond Quality Monitors

Intel uses a variety of techniques for measuring the quality and reliability of bonds. The most frequently used techniques are:

- Visual inspection
- Bond pull
- Shear test
- Infrared microscopy
- Bond etching
- Electrical testing
- Bake test
- Thermal cycle/thermal shock testing

VISUAL INSPECTION

Visual inspection is used to determine bond quality problems such as smashed bonds, skinny bonds, misplaced and deformed bonds, as well as wire conditions. It also determines metal surface conditions, including corrosion, cracks, voids, contamination, and extent of plastic deformation.

BOND PULL

The bond-pull strength test is a primary method used by Intel for optimizing the bonding window schedule and quality. The pull test is a relative test for a particular package configuration. Test results include bond strength and mode of failure.

SHEAR STRENGTH

Intel optimizes bond schedule by using the shear strength test, which is independent of wire condition and measures bond strength. The failure mode and bond strength are used as measures of bond quality and reliability.

INFRARED MICROSCOPY

Intel uses the reflective infrared microscopy (IR) technique to inspect the integrity of bond pad structure. This technique eliminates the need for decapping and accessing the die surface.

ELECTRICAL TESTING

Electrical testing measures the increase in ohmic resistance of bonds as a result of intermetallic compound and void formations, thus determining the effect of different materials and bonding process parameters on bond reliability.

BOND ETCHING

Bond etching measures the condition of layers under the bond pads. With this technique, the ball (wire) and pad metallization is removed, and the condition of underlayer materials is examined. Bond etching is useful for determining the weakest link in underlayer materials by identifying the initiation and propagation of cracks in underlayer materials.

BAKE TEST

Bake test measures the effect of intermetallic compound formation and Kirkendall voiding at wire/metal surface interfaces on bond reliability.

THERMAL CYCLE/THERMAL SHOCK TESTING

Thermal cycle and thermal shock testing are used to accelerate any possible bond pad fracture, bond lifting, and metal lifting due to bonding process deficiency or package configuration.

SURFACE ANALYSIS

Surface analysis techniques such as energy-dispersive X-ray analysis (EDX), wave-length dispersive X-ray analysis (WDX), Auger, and scanning electron microscopy (SEM) are the tools Intel uses to identify (1) the presence of contamination, (2) extent of intermetallic compound formation, and (3) bond irregularities. These techniques are part of our routine monitors of material parameters and failure analysis.

PLASTIC MOLDING

Advances in the technologies of molding compound chemistry and formulation, transfer molding, and package design have made it possible for Intel to manufacture highly reliable plastic component packages. Molded plastic packages have, in fact, gained a significant share of the devices we currently sell.

Composition

Molding compound is a composite material, with each component providing a set of properties critical to the overall performance of the system.

The composite matrix material used in Intel packages is an epoxy cresol novolac polymer. This crosslinked material is dimensionally stable, ionically clean, and resistant to assembly process and field-use temperatures. The composite's largest component by weight is silica filler, added to provide control of thermal expansion coefficient and thermal conductivity.

The balance of the compound consists of elastomeric toughening fillers, flame retardants, coupling agents to improve adhesion between matrix and filler, and release agents to allow removal of the product from the mold.

Molding Process

Intel suppliers provide partially reacted material in the form of pelletized powder preforms. The epoxy is processed in a transfer molding press, which drives the compound through the heated mold. The viscosity of the molding compound decreases as it comes in contact with the heated mold, allowing it to flow easily around the bonding wires and to fill the package cavity. Viscosity increases as the curing reaction takes place, until the compound is hard enough to be removed from the mold. An extended post-mold cure is used to ensure optimum mechanical properties in the molded package.

Molding process parameters such as cure temperature, compound transfer rate, and cure time are controlled to ensure quality and reliability in the molded part. Of equal importance are the designs of the mold runner and gate systems, the path through which the molding compound enters the package cavity. Intel uses design of experiments (DOE) methodologies that include these variables throughout the development and optimization of the molding process.

Performance/Engineering Considerations

The molded plastic package is a composite system made up of the following:

- A copper alloy or Alloy 42 lead frame
- Polymeric die attach adhesive
- Silicon chip
- Gold bonding wires
- Epoxy molding compound

Each of these components has a unique set of physical properties, and mismatches such as those in the coefficient of thermal expansion present a challenge to maintaining the mechanical integrity of the bulk materials and the interfaces between them.

Because of different rates of expansion and contraction, stresses concentrate at the interfaces between materials during the temperature excursions typical of accelerated reliability testing and circuit board mounting. When these stresses exceed the interfacial strength between materials, loss of adhesion can occur. The presence of absorbed moisture in the molding compound exacerbates this phenomenon. The following approaches are taken to prevent failure of the encapsulant during processing, testing, and end use.

From the material perspective, the supplier of the molding compound synthesizes the polymer to exhibit minimum moisture absorption. In addition, coupling agents are used to maximize adhesion between the epoxy matrix and silica filler to limit moisture ingress. Optimization of other material properties, such as flexural strength, modulus, and toughness, ensures that the material can perform under severe temperature-cycling conditions without the occurrence of cracking, which can lead to the ingress of corrosion-causing contaminants. The molding compound contains elastomeric toughening agents that curtail the growth of cracks should they begin. These “low-stress” materials also provide protection to the fragile chip surface by preventing cracking and shear deformation of the thin-film structures that make up the circuitry.

Careful package and process designs also ensure integrity of the molded package. Package engineers employ design features that provide robustness to the component by creating mechanical locks between molding compound and lead frame. Assembly process engineers design material flows that maximize adhesion and limit exposure to moisture during the manufacture, shipping, and board mounting of the component.

LEAD FINISH

Intel provides four basic lead finishes:

- Gold Plate
- Tin Plate
- SolderCoat
- SolderPlate

Each type of lead finish offers advantages for specific applications and for internal processing.

Gold Plate

The gold-plated finish is recommended for socket applications only. The packages most often involved are the ceramic laminate family, including pin grid arrays (PGAs), side-braze dual in-line packages (DIPs), and both leaded and leadless chip carriers.

Not long ago, gold was considered a universally superior lead finish because of its solderability, and electrical and nonoxidizing properties. During the past several years, however, it has been determined that soldering gold-plated component leads directly into a PC board has clear disadvantages. Excess gold in the solder joints can result in the formation of a brittle alloy, causing the joints to fail over time in high-vibration or board-flexing environments.

For example, in military applications requiring leadless chip carrier mounting, such considerations become critical. Currently, military requirements demand that a solder coat replace gold in direct soldering uses for both leadless and leaded components. Gold plating remains the lead finish of choice for socketed units.

Tin Plate

Intel uses tin plating for selected ceramic DIP (CERDIP) packages only. The tin-plated finish can be either directly soldered or socketed with a non-gold socket contact finish.

Tin offers the advantage of a slightly higher melting point (232°C) than solder (180°C), and it can be burned in at higher temperatures without melting. However, when compared to solder coating, tin plating does not age as well in long-term storage from the standpoint of solderability. This may occur because tin plating is more porous than solder coating. In general, pure tin plating is more susceptible to tin whisker growth under certain mechanical and environmental conditions.

SolderCoat

SolderCoat component leads offers the distinct advantages of a low melting point (180°C) and resistance to aging.

The composition of SolderCoat is the eutectic alloy of 63% tin and 37% lead. Intel normally applies the coating in the following sequence: (1) cleaning the leads, (2) applying a flux, (3) dipping the leads into molten solder, and (4) finishing with a hot water rinse. Great care is taken to minimize any thermal shock to the package and die during SolderCoat processing and cleaning of the unit after coating.

Intel provides SolderCoat lead finish on all plastic and ceramic DIPs, all military packages, and some selected plastic leaded chip carriers (PLCCs). The customer can use this lead finish in a variety of PC board assembly processes, including wave soldering, infrared, and vapor phase.

SolderPlate

Intel uses tin-lead alloy plating for plastic quad fine-pitch, quad flatpack, and PLCC packages.

The codeposited elements form an alloy composition of approximately 85% tin and 15% lead. As shown in Figure 3-9, the plating on the packages' copper lead frames, with a thickness of 200 microinches minimum, provides full coverage of the copper without exposing any formed intermetallics to the air. At the same time, SolderPlate produces a very solderable finish with a melting point of approximately 215°C. Like tin-plated leads, those plated with tin-lead alloy can be directly soldered using infrared or vapor phase methods, or socketed.

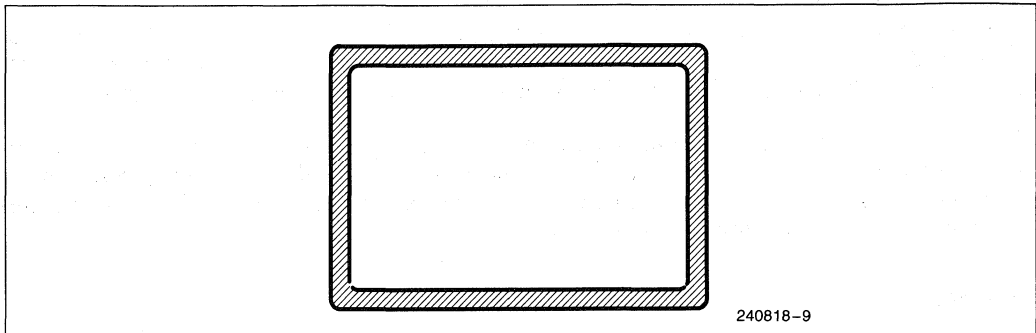


Figure 3-9. Tin or SolderPlating on a Lead Frame

Lead Finish Process Flow

The following sections illustrate the process flow for each type of Intel lead finish.

GOLD

Packages with this finish are purchased from the package vendor as raw piece parts.

SOLDERPLATE

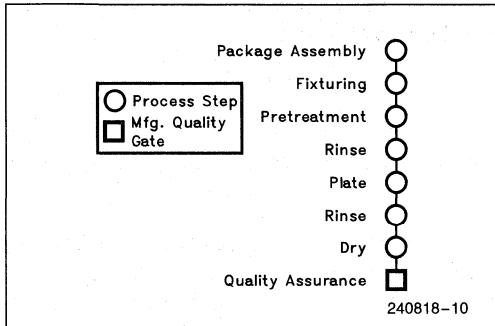


Figure 3-10. Process Flow for Tin and SolderPlating

SOLDERCOAT

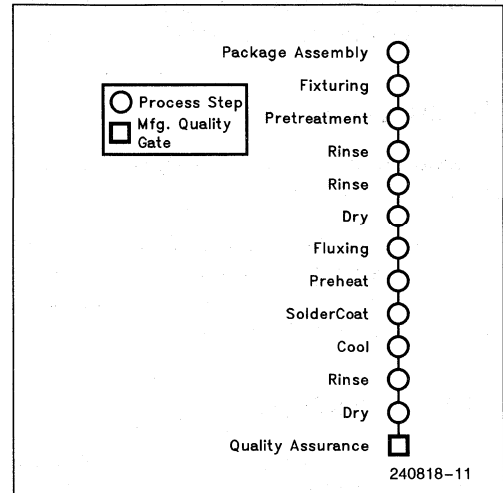


Figure 3-11. Process Flow for SolderCoat

3

Process Controls

Plating operations are controlled by monitoring a combination of several items:

- Physical arrangement and condition of the plating anodes and fixtures, as well as distance to the work to be plated

- Chemical analysis of plating and pretreatment solutions for all constituents and contaminants, including by-products
- Plating parameters such as temperatures, rinse flows, voltage and current density, and process times

SolderCoat operations are controlled and monitored for many of the same items as plating:

- Physical height of the solder and condition of fixtures
- Chemical analysis of the pretreatment solution and solder
- Operational parameters such as conveyor speed, flux density, preheat temperature, solder temperature, thermal package profiles, and rinse flows and temperatures

Product Controls

In addition to process controls, Intel continues to monitor IC lead-finish functionality using a series of product tests.

Lead-finish thickness and solderability monitors are performed on all products. Intel has also developed a supplementary solderability test to track long-term trends. Alloy thickness and composition are tested in the tin-lead plating operations on a real-time basis. Selected products are also tested for wetting speed.

LEAD FORMING

Lead forming is a twofold assembly operation that bends and trims plated or solder-dipped leads to meet specified dimensional accuracy. Leads can be formed into three standard configurations: gull-wing and J-lead for surface mount packages, and straight form for through-hole mounting. During the forming process, extreme care is taken to expose the tin-plated or solder-coated leads to minimum stress and abrasion, thus ensuring maximum strength and reliability.

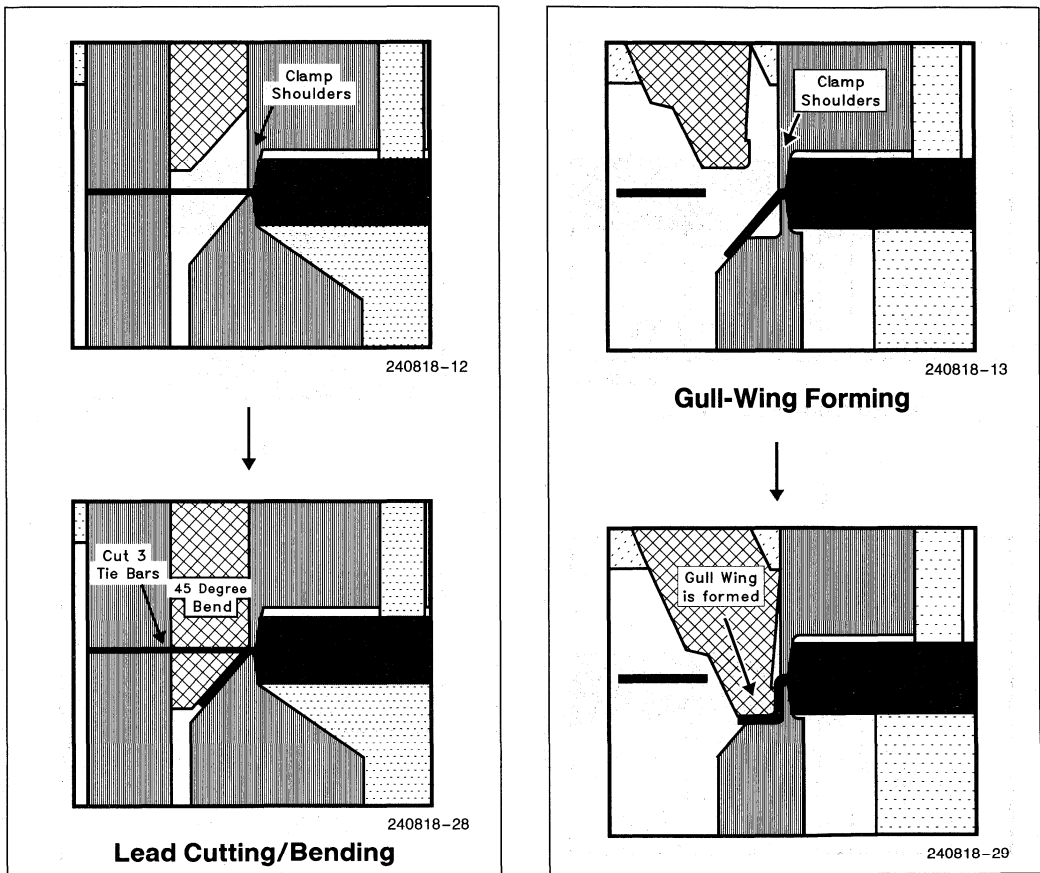


Figure 3-12. Formation of Gull-Wing Leads

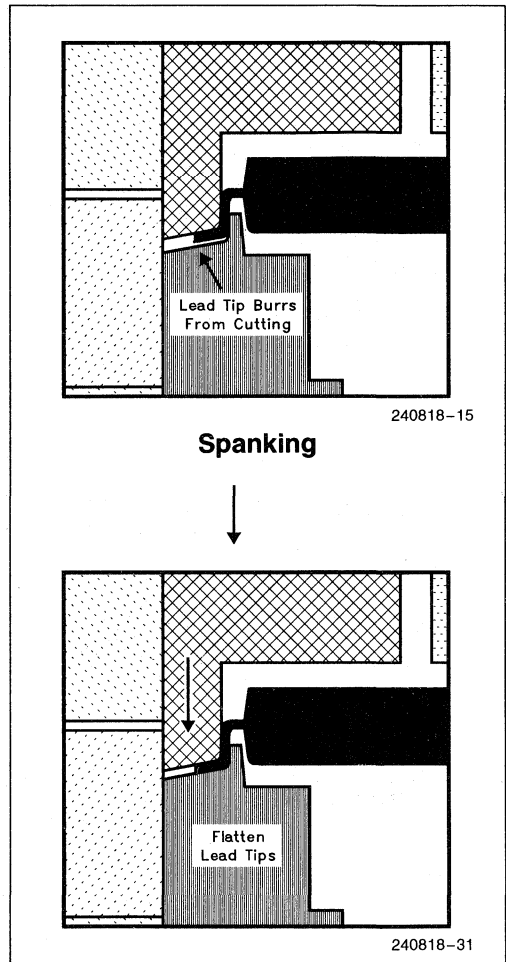
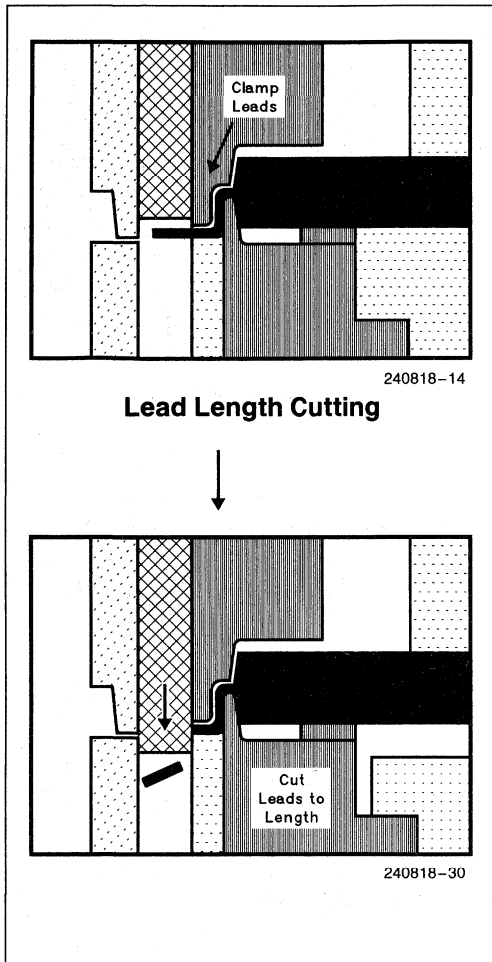
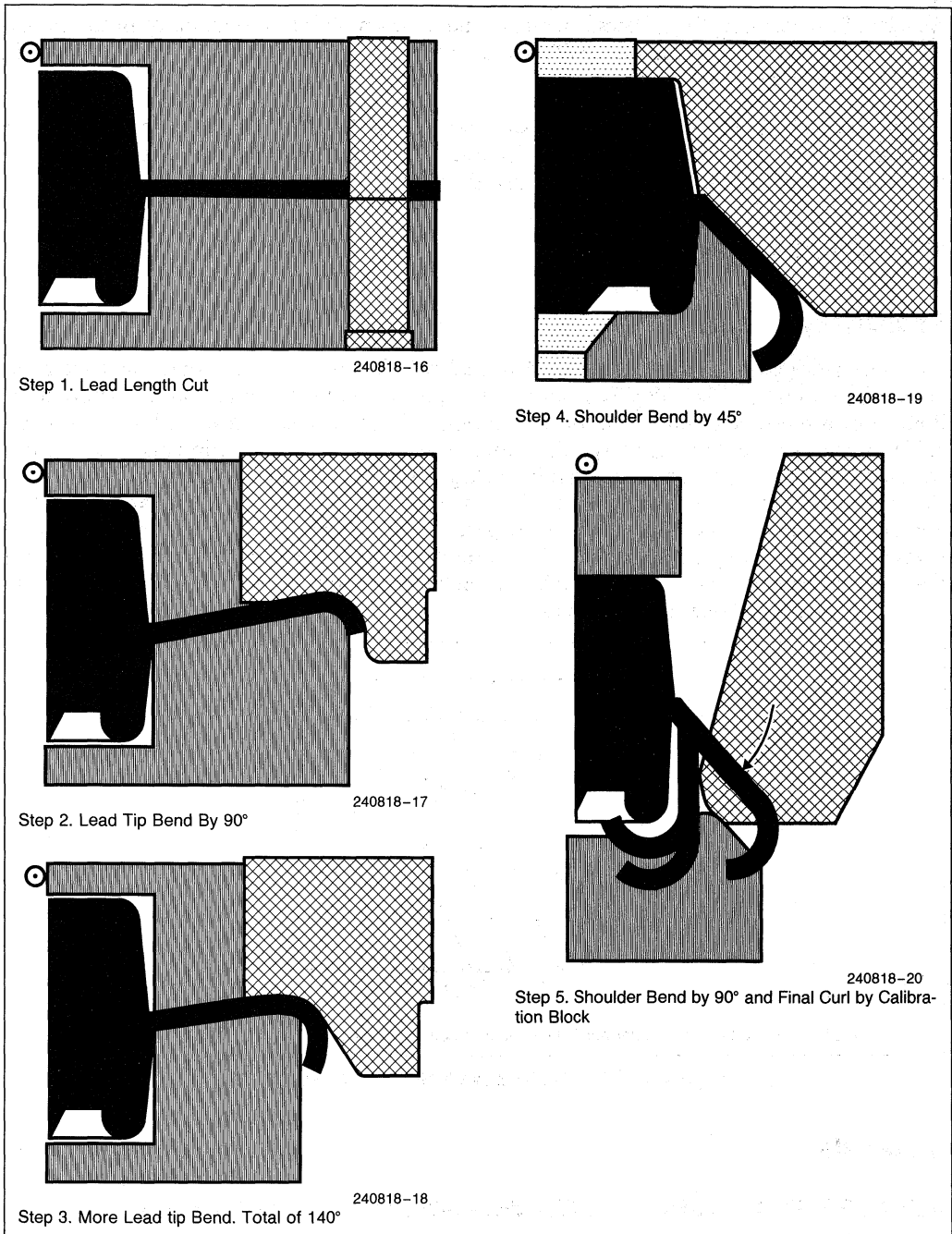


Figure 3-12. Formation of Gull-Wing Leads (Continued)



3

Figure 3-13. Deflash, Trim, and Form of J-Leads on PLCCs

As part of the lead-forming process, dambars and excess molding compound or flash that has flowed between the leads and out to the dambars are removed simultaneously from the leads. This step electrically isolates the leads.

Finally, individual units are separated or singulated from the lead frame at the tie bar support and carefully placed into tubes or trays for lead protection. Singulation is either combined with the forming operation or occurs separately after forming.

HERMETIC SEALING

Packaging Options

Hermetic sealing of IC packages is used to seal the silicon electronic component from the external environment, specifically from water vapor and contaminants that can shorten the lifetime of a sensitive electronic device. Two types of hermetic seals are used at Intel: hard-solder precious metal brazing alloys (the laminated ceramic package family) and low melting-temperature glasses (the pressed ceramic package family). The metal-sealed packages are of the laminated ceramic type and involve the brazing of a metal lid to a gold-plated thick-film seal ring on the ceramic. The glass-sealed packages utilize glass to create the seal between pressed ceramic pieceparts. Figure 3-14 illustrates the relative hermeticity of various sealing materials. It can be seen from the graph that metal seals provide the highest levels of hermeticity, followed by glasses and ceramics.

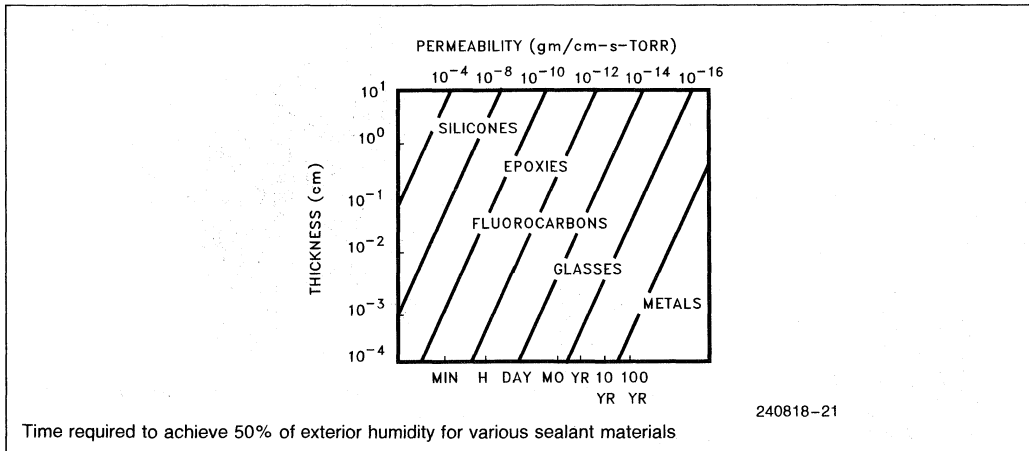


Figure 3-14. Relative Hermeticity of Materials

Materials

METAL-SEALED LAMINATED CERAMIC PACKAGES (CX PACKAGES)

Of the two hermetic package families, metal-sealed packages provide higher levels of hermeticity and reliability. At Intel, the metal-sealed packages utilize a gold-tin eutectic hard solder to create the hermetic seal. The composition of the alloy is 80% gold, 20% tin, and has a

melting point of 280°C (see Figure 3-15). This solder was chosen for its excellent wetting characteristics to the seal ring and lid materials, as well as its high resistance to thermal fatigue. Seals created by the Au-Sn alloy can withstand thousands of condition C thermal cycles without failure.

The gold-tin eutectic seal is made to a seal ring on the surface of the aluminum oxide ceramic. The seal ring is composed of a tungsten thick film that is fired to the ceramic material and plated with a thin nickel diffusion barrier and a gold overplate. The gold overplate prevents oxidation and provides a wettable surface for the solder. Figure 3-16 is a schematic of the seal area.

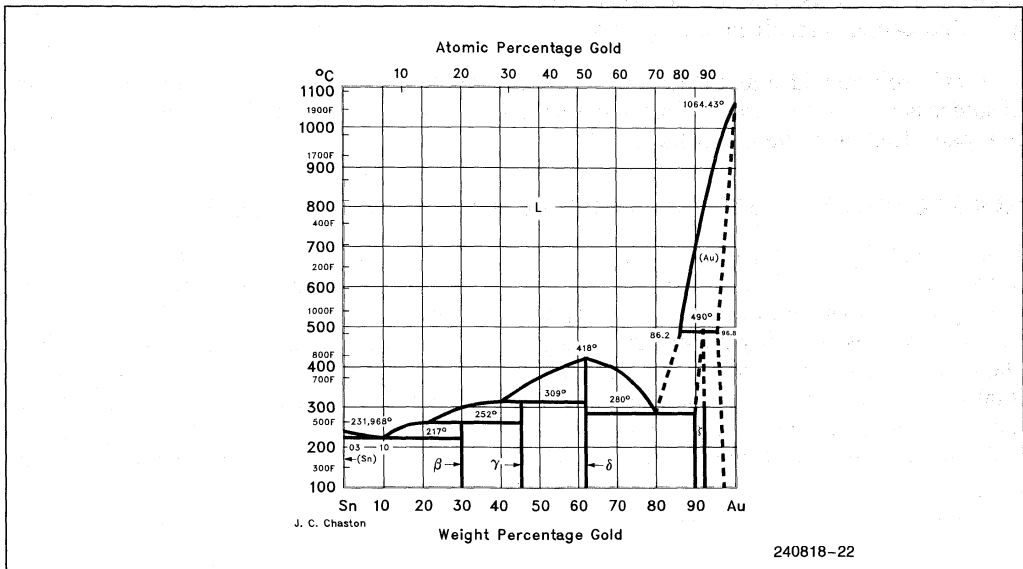


Figure 3-15. Au-Sn Phase Diagram

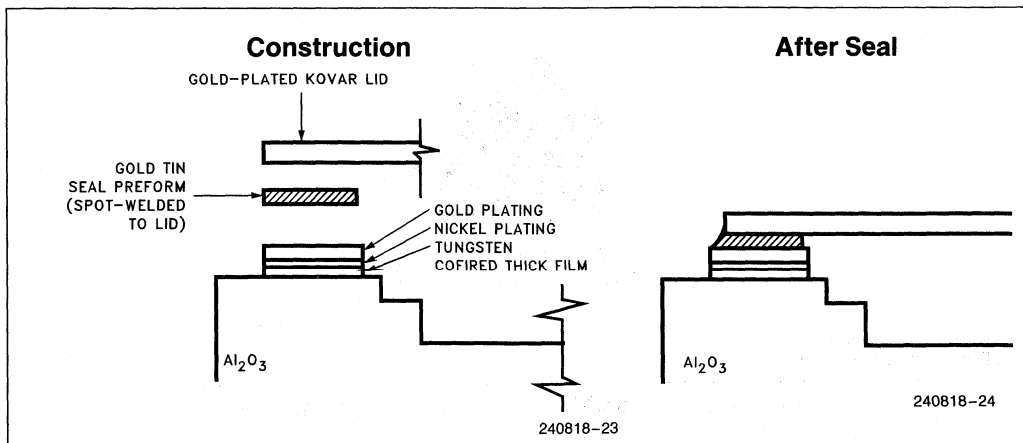


Figure 3-16. Schematic Cross-Section of a CX Package Seal (Thicknesses Not To Scale)

The lid material is gold-plated kovar (a nickel-iron alloy with low thermal expansion) to which is attached an 80% gold, 20% tin alloy (eutectic composition) preform. The seal preform is attached by spot welding. The lid material was chosen for its stiffness and because the thermal expansion of kovar is close to that of aluminum oxide ceramic. The stiffness prevents damage during testing, and the low thermal expansion minimizes stress at the seal due to thermal expansion mismatch.

The thicknesses of the plating used in the seal ring area are important to the success of sealing using this system. The thickness of the gold must be controlled to prevent premature nickel diffusion and oxidation at the gold surface, which can create a poorly wetted surface that will result in seal defects. The nickel diffusion barrier prevents the interdiffusion of tungsten and gold that can also result in seal defects.

The seal preform width and thicknesses are also specified to ensure that an adequate amount of solder is present to create a continuous seal. Too large a preform can result in excess solder that can bleed onto the lid surface.

GLASS-SEALED PRESSED CERAMIC PACKAGES (DX PACKAGES)

In glass-sealed packages, a ceramic lid is sealed to the base ceramic with a vitreous (noncrystallizing), lead-based glass having a low melting temperature. The glasses chosen for hermetic sealing are lead-zinc borates that generally seal in the 415-450°C range. Figure 3-17 illustrates the vitreous glass-forming region (region A) in the lead-zinc-borate system from which these glasses are chosen. The glasses used in the industry have compositions in this range, with the final selection based on obtaining the lowest possible processing temperature. As a result, the most commonly available seal glasses have very similar compositions. The glasses are highly resistant to chemical plating baths (see Table 3-5) and have excellent thermal shock resistance.

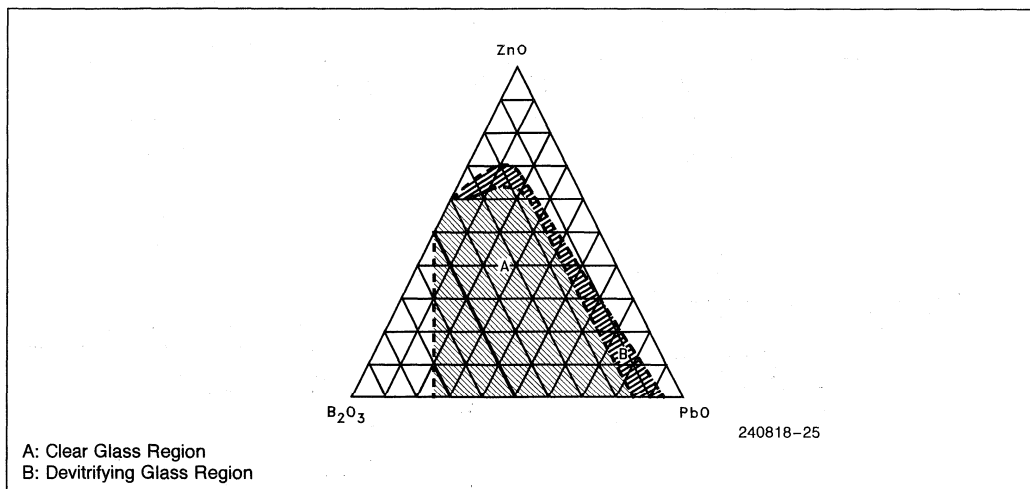


Figure 3-17. Lead-Zinc-Borate Phase Diagram

Table 3-5. Chemical Durability of Glasses

Chemical Treatment	Glass Type			
	Intel	B	C	D
50% H ₂ SO ₄ 95°C, 1 hr.	8.65	2.32	5.89	0.88
50% H ₂ SO ₄ 25% HNO ₃ 25°C, 5 min.	2.37	2.12	2.11	1.50
5% HNO ₃ , 25°C Direct Transfer to 50% H ₂ SO ₄ at 95°C for 15 min.	80.9	96.4	56.7	62.7

*Glasses must exhibit chemical durability in order to withstand the lead-plating baths.

The glasses used for package sealing have high thermal expansions relative to the ceramic. To reduce thermally induced package stresses, it is necessary to reduce the thermal expansion of the glasses by adding low-thermal-expansion fillers. These fillers are chosen to be compatible with the lead glass and do not react during processing.

3

Because the glasses all have similar compositions, they have similar strengths. Table 3-6 lists the measured bending strengths for several different sealing glasses commonly used. The glass used by Intel can be seen to have bending strengths equivalent to other commonly used glasses. The fracture toughness of Intel's sealing glass is also found to be quite similar. It is expected that the mechanical performance of Intel's sealing glass will be equivalent to other commonly used glasses.

Table 3-6. Bending Strengths and Fracture Toughnesses of Several Lead-Based Sealing Glasses

Glass	Four Point Bending Strength (MPa)	Fracture Toughness (MPa√m)
Intel	20.1	1.0
B	21.4	1.1
C	20.0	0.9

Figure 3-18 is a schematic cross-section of a glass-sealed package.

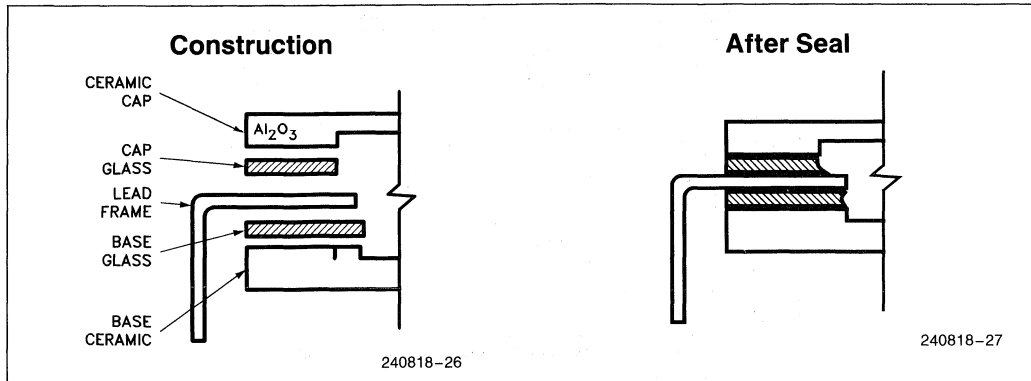


Figure 3-18. Cross Section of a Glass-Sealed Package

Processes

LAMINATED CERAMIC PROCESSING

Sealing of metal-sealed packages is accomplished in a continuous belt furnace. The metal lid is aligned and clipped in place to ensure that the seal ring and preforms remain properly aligned and that sufficient pressure is exerted on the lid to ensure good contact. The units are ramped in temperature past the melting temperature of the alloy and allowed to soak at the sealing temperature. The soak time allows the molten metal time to wet all the sealing surfaces sufficiently and to form an integral metallurgical bond with the seal ring and lid plating.

Sealing can be accomplished in either an inert (nitrogen) or reducing atmosphere (forming gas N_2H_2). The seals obtained with either atmosphere are equivalent in performance. The reducing atmosphere is used to build additional margin into the sealing process.

The sealing process is controlled by monitoring the seal temperatures with a thermocouple embedded in a package and passed through a fully loaded furnace. This ensures that the furnace profile obtained is representative of that seen by actual product. Water vapor content of the sealing atmosphere is also controlled to ensure that the final internal-cavity water vapor levels meet the industry requirements.

PRESSED CERAMIC PROCESSING

Glass-sealed packages are also sealed in a continuous belt furnace. For these packages, caps are aligned to the base with fixtures as the units pass through the furnace, and no clips are used; the weight of the package is sufficient to create the seal. Because glass does not have a sharp melting point, it is necessary to hold the units at the seal temperature for sufficient time to allow the glass to flow and wet the metal lead frame and ceramic, and thus create the final seal. Insufficient time will result in noncontinuous seals or incomplete flow, causing glass depressions between the leads. These depressions in their worst form can create a continuous

path to the cavity (nonhermeticity), or in less severe cases act as a stress riser and result in package damage during subsequent handling. Sealing is performed in an oxidizing ambient (dry air) to prevent reduction of the lead glass.

As with the metal-sealed packages, the process is controlled by profiling a fully loaded furnace by means of a thermocouple embedded in a CERDIP-type package, again to get an accurate representation of the actual sealing conditions. Water vapor content and flow rates of the atmosphere are controlled to ensure that the internal-cavity water vapor requirements are met.

Performance

Intel's hermetic packages are tested individually for hermeticity using two tests: fine and gross leak. Two tests are required, since neither test can adequately detect the entire range of leak sizes. Fine leak uses either radioactive tracer gases and a scintillation counter or helium and a mass spectrograph to identify fine leaks. Larger leaks do not show up, as the gases leak out too quickly for the detectors to identify. The industry-acceptable leak rate for hermetic packages is less than 5×10^{-8} Std. CC atm/min.

Gross leak testing, which identifies larger leaks that fine leak cannot detect, uses a high-vapor pressure fluorocarbon liquid as the detection medium. The unit is pressurized in a container of the fluorocarbon to force the liquid into the leak. After pressurization, the unit is immersed in a hot bath, which vaporizes the fluorocarbon trapped in the leak. A steady stream of bubbles indicates the location of the leak. The gross leak test cannot be used for small leaks, as the liquid will not penetrate leaks smaller than a certain size.

Performance Characteristics of IC Packages

4



CHAPTER 4 PERFORMANCE CHARACTERISTICS OF IC PACKAGES

IC PACKAGE ELECTRICAL CHARACTERISTICS

The following parameters are provided for Intel packages:

- DC resistance (R) of leads or pins
- Capacitance (C), including lead-to-lead and loading capacitances
- Inductance (L), including only self-inductance values for pins or leads

These parameters can be experimentally measured and theoretically calculated. The package parameters for the following package families are representative of measured, or calculated, values:

- Plastic quad flatpack (PQFP)
- Multilayer molded package (MM)
- Ceramic quad flatpack (CQFP)
- Pin grid array (PGA)

The MM, CQFP, and PGA packages can be designed with ground and power planes. Since these packages are custom-designed for each product, their parameters may not reflect the actual values for a particular product. The actual parameters can be obtained by contacting Intel.

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For electrical parameters of packages not listed in the tables, please contact your local Intel field sales engineer.

Package Electrical Data

Following are the electrical characteristics of Intel's PGA packages. The three parameters discussed are D.C. resistance (R), capacitance (C), and inductance (L). A summary of typical ranges of values is presented in Table 1.



Table 4-1. Summary of PGA Electrical Data

Lead Count	I/O Lines				Power and Ground		
	L (nH)	C _L (pF)	C _{LL} (pF)	R** (mΩ)	L (nH)	C (pF)	R (mΩ)
68(S)	9-13*	2-3	2-3	200-300	9-13‡	2-3	200-300‡
68(M)	5-9	2-3	≤0.5	200-300	2-4	≥75	50-100
88(S)	9-14*	2.5-4	2.5-4	220-350	9-14‡	2.5-4	220-350‡
88(M)	5.8-8.6	2.5-6	≤0.5	220-350	2-3	≥121	50-100
132(M)†	6-11	6-15	≤0.3	220-700	0.5-3.9	300-900	20-50
168(M)	9-22	4-9	≤0.5	220-800	0.5-1.0	300-900	20-50

NOTES:

*Ground and trace are separated by 0.100".

†Optimized package design.

**Resistance of the gold wire (65 mΩ-70 mΩ for 100 mil length) is not included.

‡Single lead. For multiple leads divide the tabulated value by the number of leads.

Measurement Errors: L values are ±0.3 nH

C values are ±0.1 pF

R values are ±5 mΩ

DEFINITIONS:

S — Single Layer (No Power and Ground Planes)

M — Multi-Layer (With Power and Ground Planes)

C_L — Loading capacitance

C_{LL} — Lead to lead capacitance

Table 4-2. Summary of CQFP Electrical Data

Electrical Parameter		Lead Count	
		164L	196L
L _{Lead}	nH	3.3	3.3
R _{Lead}	Ω	0.004	0.004
L _{Trace (I/O)}	nH	5.0	6.0
R _{Trace (I/O)}	Ω	0.8	0.9
C _{Load}	pF	4.0	5.0
L _{Trace (V_{CC}/V_{SS})}	nH	1.5	2.5
R _{Trace (V_{CC}/V_{SS})}	nH	0.2	0.4
L _{Wire}	nH	3.0	3.0
R _{Wire}	Ω	0.08	0.08
C _(V_{CC} Plane to V_{SS} Plane)	pF	170.0	240.0

Table 4-3. Summary of MM Packages

Electrical Parameter	Lead Count		
	132L	164L	196L
$L_{(I/O)}$ [nH]	14.0	16.0	18.0
$R_{(I/O)}$	<0.1Ω	<0.1Ω	<0.1Ω
C_{Load} [pF]	<2 pF	<2 pF	<2 pF
L_{Lead} (V_{CC} or V_{SS}) [nH]*	7.0	7.0	7.0
L_{Wire} (V_{CC} or V_{SS}) [nH]*	3.0	3.0	3.0
R_{Wire} (V_{CC} or V_{SS})	<0.1Ω	<0.1Ω	<0.1Ω
$C_{(V_{CC} \text{ or } V_{SS}, \text{ Plane to Plane})}$ [pF]	90.0	140.0	210.0

NOTE:

* To calculate effective inductance and resistance of V_{CC} or V_{SS} :

$$L_{eff} = \frac{L_{Lead}}{\# \text{ of leads}} + 0.1 + \frac{L_{Wire}}{\# \text{ of pads}}$$

$$R_{eff} = \frac{R_{Wire}}{\# \text{ of pads}}$$

Table 4-4. Summary of PQFP (iMP) Electrical Data

Electrical Parameter	Lead Count				
	84L	100L	132L	164L	196L
R (MΩ)	70–80	70–80	70–80	70–80	70–80
L (nH)	5.8–6.6	6.1–7.1	7.3–8.5	8.0–14.5	9.0–15.5
C (pF) (Loading)	<1.0	<1.5	<2.0	<2.2	<2.3
C (pF) (Ld/Ld)	<0.5	<1.0	<1.5	<1.5	<1.6

Electrical Parameters

D.C. RESISTANCE (R)

The D.C. resistance is normally the cause of IR voltage drops. Reduction of D.C. resistance is particularly important in the ground and power paths. The relatively high resistance of the traces in the ceramic package is due to material and geometry (thickness, 0.001 in.; width, 0.006 in.; and various lengths). The resistance per square centimeter of tungsten used is 0.010Ω.

CAPACITANCE (C)

Capacitance is determined by the (1) length of the leads, (2) distance separating the leads, (3) dielectric constant of the material between them, (4) lead thickness, and (5) number of leads involved. Larger leads have larger values of capacitance. The relative dielectric constant of the material used for ceramic PGAs is in the range of 8-10. The dielectric constant for plastic package material is around 4-5.

Capacitance is classified as “loading” or “lead-to-lead”. The loading value represents the capacitance of a single lead in the presence of a system of conductors. It is greater than the lead-to-lead value, which represents the capacitance between two leads with all other conductors grounded. The loading capacitances are the diagonal terms in the C matrix, and lead-to-lead capacitances are the off-diagonal terms.

INDUCTANCE (L)

The inductance value is influenced by the package size and the location of the leads in a given circuit with respect to the power and ground locations. The inductance of the I/O lines is due to the circuit loop created by the current-in and current-out paths. If the loop area is smaller, effective inductance is also smaller. Shorter, wider leads have smaller values of inductance. For multiple switching, the concept of a loop breaks down and must be replaced with the inductance matrix, which consists of self-inductance and mutual inductance. For multilayer packages with power and ground planes, the problem is not severe, because the mutual inductance (off-diagonal) terms in the matrix are small compared to the self-inductance (diagonal) terms.

THEORETICAL CALCULATIONS

The theoretical values for package parameters are obtained by using an Intel proprietary software package called iPEST (Intel Package Electrical Simulation Tool). This software calculates the inductance, capacitance, and resistance values from the CAD-based geometry information and material properties.

For single-layer packages without power and ground planes, the complete inductance matrix for the leads can be calculated. The software computes the parameters for each component of the package, such as trace, lead, bond wire, pin.

Measurement Methods

RESISTANCE

The resistance for a given package is measured from the tip of the bond finger to the pin braze pad. The lead resistance for plastic packages is measured from tip to tip.

Figure 4-1 shows the four-probe set-up used to measure the resistance values. Two sets of readings are taken by reversing the direction of current to eliminate the contact potential. The average value is considered the resistance of the sample.

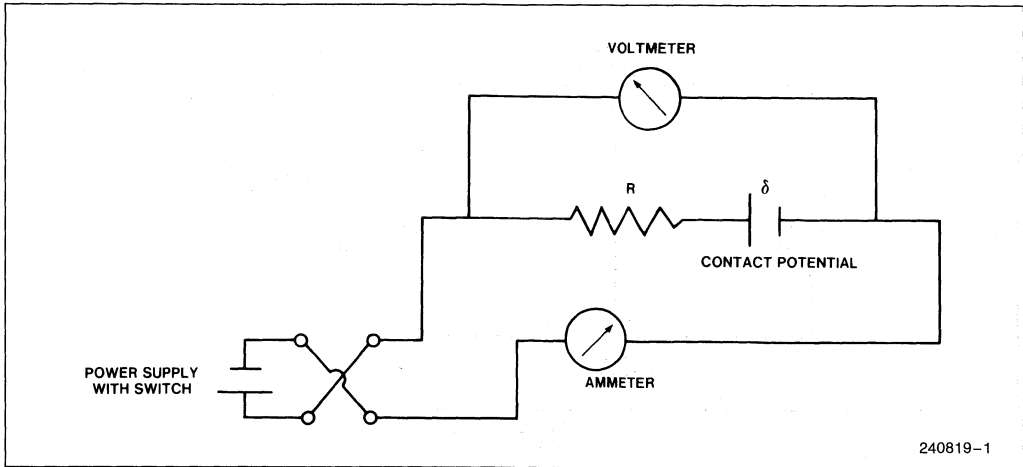


Figure 4-1

CAPACITANCE

Capacitance measurements are made using two separate methods. The first method measures the capacitance of a single lead in the presence of a system of conductors (loading capacitance). In this method, all leads except one are grounded and then the capacitance of the remaining lead is measured with respect to ground, as shown in Figure 4-2.

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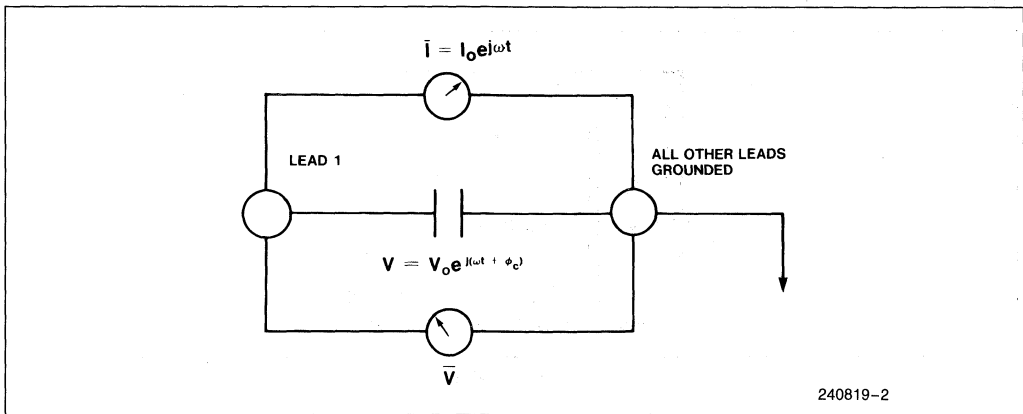


Figure 4-2

In the second method, shown in Figure 4-3, all the leads except two are grounded, and the capacitance is measured between the two leads (lead-to-lead capacitance). In the presence of a ground plane, the lead-to-lead capacitance is very small compared to the loading capacitance. If the ground plane is kept floating, the lead-to-lead capacitance is normally very close to the loading capacitance.

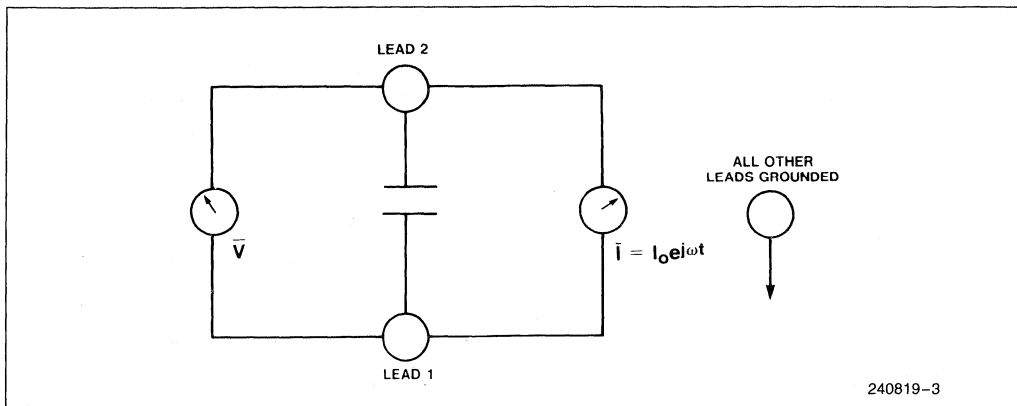


Figure 4-3

The measurements are performed using a current source having frequency f and then by measuring the voltage drop and phase shift across the sample. For pure capacitance, the phase shift is $(-\pi/2)$.

INDUCTANCE

As shown in Figures 4-4 and 4-5, the inductance is measured in a circuit that includes internal wires bonded from each of two arbitrarily chosen leads to a metal plate on the die pad (in place of a silicon chip).

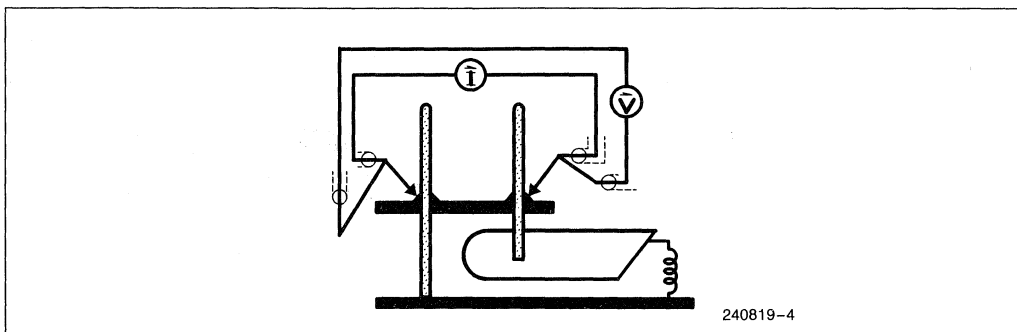


Figure 4-4

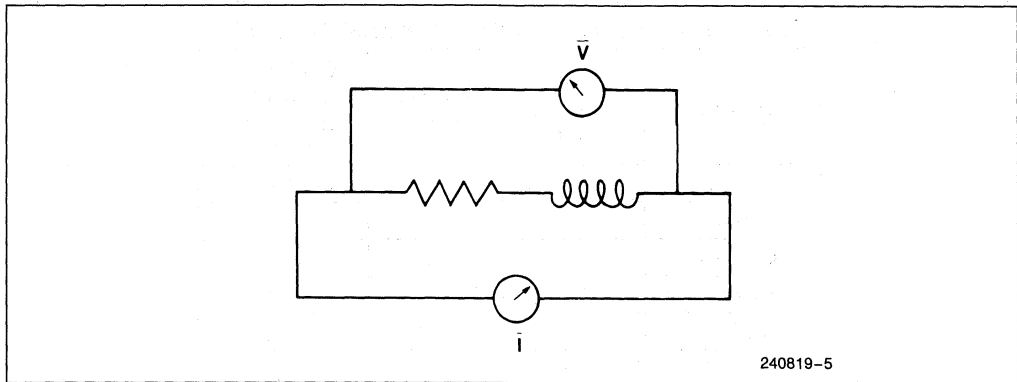


Figure 4-5

For I/O lines, the current enters the trace and is distributed in the ground plane. The interaction of the current in the trace with the current distributed in the ground plane determines the effective inductance. In PGA packages, the magnetic field is primarily contained in a plane perpendicular to the X-Y plane containing the I/O trace. This helps to keep the mutual coupling between two traces to a minimum.

Like capacitance measurements, inductance measurements use a current source having frequency f . By measuring the voltage drop and the phase shift across the sample, one can determine the inductance. For a pure inductive circuit, the phase shift is $(+\pi/2)$.

4

IC PACKAGE MECHANICAL CHARACTERISTICS

Sources of Stress

Each assembly step is a potential stress-inducing operation: Silicon chipping and metal peeling can occur during the saw process; die backside damage and chipping during the die attach process; bond pad and silicon substrate damage during wire bonding; and wire bond sweep during encapsulation (plastic packages).

In addition, accelerated environmental stress tests can introduce failure modes that require detailed modeling to provide satisfactory interpretation of the results and extrapolation to failure rates in the field. These accelerated tests include thermal cycling to produce repeated thermal stresses, and shock and vibration to produce dynamic and oscillatory mechanical loads on the package and its contents.

The ability of the package to withstand these stress-inducing environments is governed by the properties of the materials used in construction, as well as by the design geometry. The key material properties are (1) elastic modulus, (2) density, and (3) linear coefficient of thermal expansion (CTE). The modulus is required in all models, while density is needed in dynamic analyses, and CTE is needed in thermal analyses. These properties are listed in Table 4-5 for key packaging materials. Commonly referenced geometric design variables include length (L) and thickness (h) of elements making up layers in the packages.

Table 4-5. Room Temperature Material Properties

Material	Elastic Modulus (GPa)	Density (kg/ltr)	Coefficient of Thermal Expansion (MC) ⁻¹
Silicon	150	2.3	4.2
Die Attach	5*	2.9	50.0*
Aluminum	70	2.7	23.0
Copper	120	9.0	17.0
Gold	80	18.9	14.3
Alloy 42	145		6.4
Molding C _{PD}	14.2*	1.80	17.0*
Al ₂ O ₃	265	3.99	5.0
Solder	8.3	9.3	26.0

NOTE:

*Below T_g, glass transition temperature (~ 100°C, die attach adhesive; -175°C, molding compound)

Stress, Strength, and Beyond

Much of Intel's stress-modeling work performed using 2-D or 3-D finite element analysis (FEA) methods is based on elastic material behavior. The limit to this behavior is governed by the type of material being analyzed. For brittle materials such as silicon, ceramics, and molding compounds, fracture initiation represents the limit to the elastic model. For ductile materials such as aluminum, copper, gold, Alloy 42, and solder, onset of plastic flow becomes the limit.

While the same 2-D/3-D stress analysis applies to both brittle and ductile materials up to their elastic limits, different stress parameters must be calculated to determine if the elastic limit has been reached. For brittle materials, the maximum principal stress, which is proportional to the sum of the normal stresses, is compared to the ultimate tensile strength or the fracture toughness. For ductile materials, the effective stress, which is a measure of the maximum shear stress, is compared to the yield strength. Representative fracture toughnesses (K_{IC}), ultimate tensile strengths (σ_u), and yield strengths (σ_y) are listed in Table 4-6. Because interfacial adhesion strengths also govern the onset of delamination, these are listed in the table for bimaterial interfaces of interest.

Table 4-6. Fracture Toughness and Ultimate and Yield Strengths for Selected Materials (Room Temperature Data)

Material	K_{Ic} (MPa m ^{1/2})	σ_u (MPa)	σ_y (MPa)
Silicon	0.8	150	
Ceramic		300	
Molding C _{pd}	2.0	100	
Aluminum (Annealed)			20
Copper Alloy			415
Gold			165
Alloy 42			275
Solder			25
Si/MC		14	
Cu/MC		7	
Al/PI	0.02		

Beyond the elastic limit, the linear stress-strain relationships must be supplemented with crack growth formulas for brittle materials and with plastic flow rules for ductile materials. The resulting constitutive equations are nonlinear and computation-intensive. They provide a mathematical description of irreversible processes that can lead to functional failures in the product if sufficient cyclic operations are completed. When supplemented with experimental data, these post-elastic solutions are useful in providing product life estimates (reliability prediction).

4

Applications

BASIC ANALYSIS

To determine thermally and mechanically induced package stresses, Intel uses both modeling and measurement methods. Modeling is carried out at three levels: (1) laminated beam analyses to establish trends as design and material properties are varied; (2) 2-D FEA when the limits of the strength of materials model are reached for configurations that can be modeled as plane stress or strain; and (3) 3-D FEA for configurations that defy simplification.

Measurement of stresses on the device surface is performed with piezoresistive elements (pressure-sensitive resistors) diffused onto the surface of the silicon device. Under stress (strain), the resistance of the elements changes and can be detected using simple bridge circuits. Comparison of predictions and measurements provides an important self-check on the two tools used for stress analysis.

Intel uses ANSYS software, a trademark of Swanson Systems Inc., for the 2-D and 3-D FEA modeling. Because it allows for nonlinear material behavior (elastic, plastic, and creep), it is a powerful analytical tool. In addition, it is widely accepted in the electronics industry and has become a de facto standard.

RESIDUAL THERMAL STRESSES IN PLASTIC PACKAGES

Die-level stresses are created during die attach for ceramic and plastic packages, and during encapsulation for plastic packages. Representative stresses are shown in Figure 4-6 for die attach and in Figure 4-7 for encapsulation.

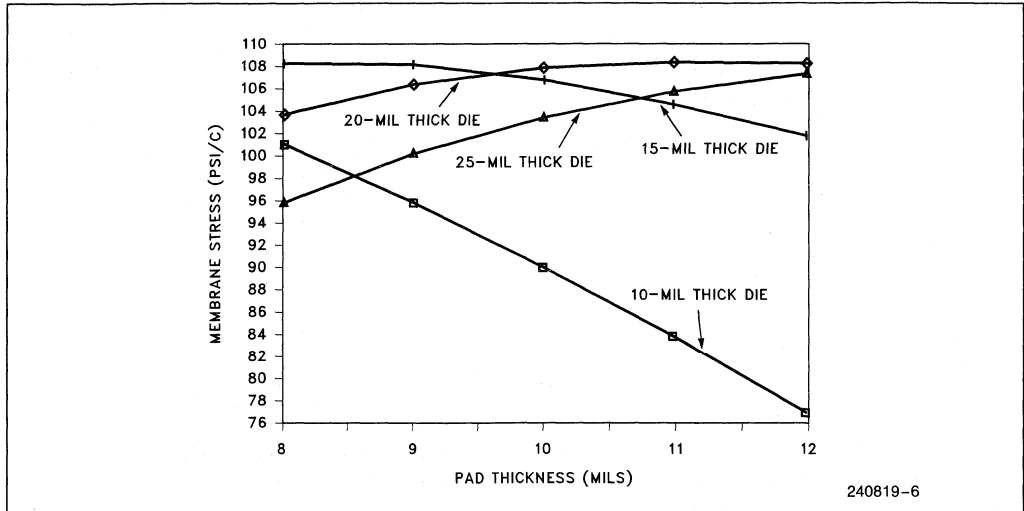


Figure 4-6a. Die and Pad Thickness Dependencies Die Surface Stresses Due to Die Attach

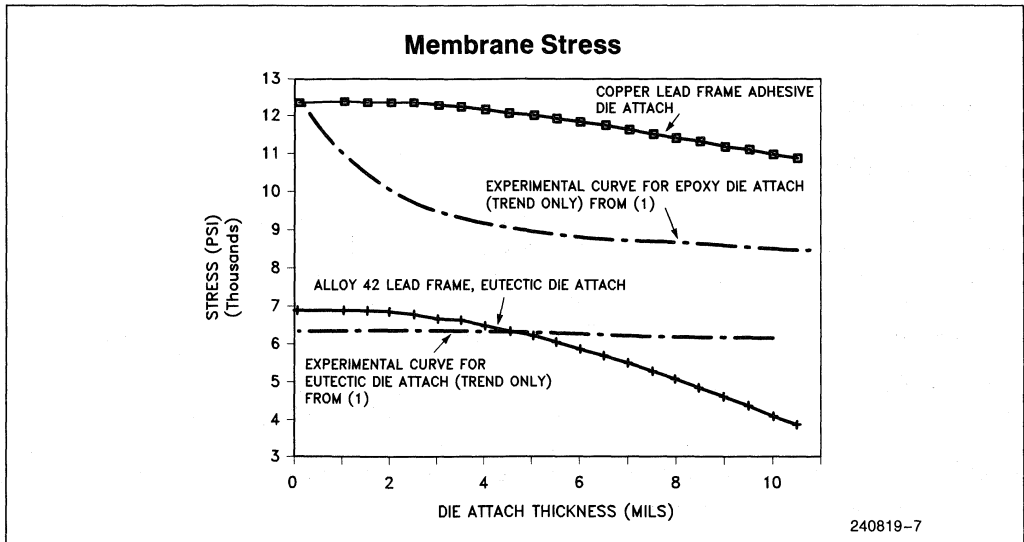


Figure 4-6b. Die Attach Thickness Dependencies Die Surfaces Stresses Due to Die Attach

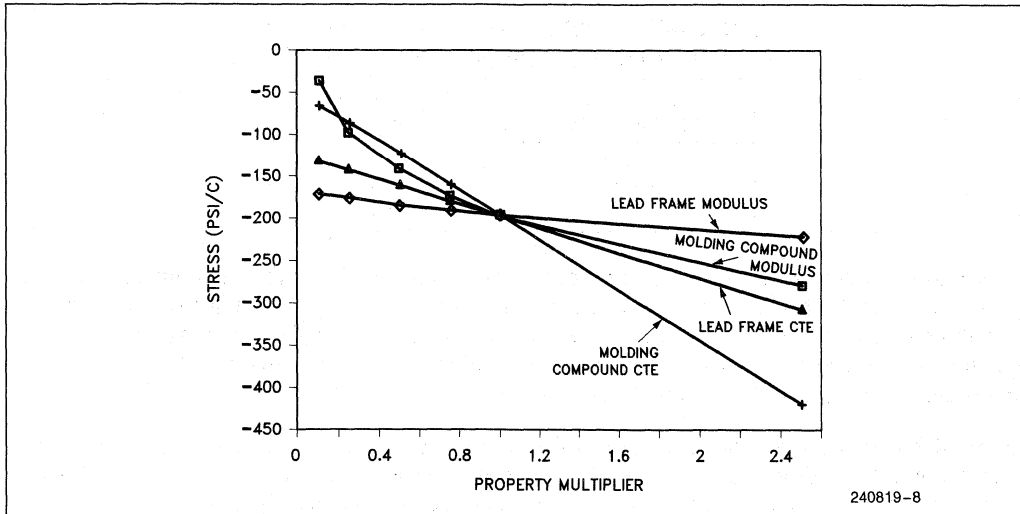


Figure 4-7. Die Surface Stress Variation with Molding Compound and Lead Frame Properties

These stress fields have been calculated using laminated beam theory and thus are applicable to regions of the die, lead frame, and package away from the edge of the laminations. Edge effects are discussed at the end of this section. The stress levels reported here are based on cooldown from the process temperature ($T \sim 240^{\circ}\text{C}$ for die attach, $T \sim 170^{\circ}\text{C}$ for encapsulation), the zero stress state, where thermal stresses arise because of differential expansion of the materials making up the beam laminations.

Shown in Figure 4-6a is the dependence of the die's top-surface stress on die, die attach, and lead frame thickness. Because the lead frame contracts more than the die during cooldown, the laminated beam bows upward, creating a tensile stress on the die's top surface. As the figure illustrates, a thick die in combination with a thin pad acts to reduce the tensile stress level. Interestingly, the converse is also true: A thin die in combination with a thick pad reduces the stress. This seemingly anomalous result is due to the reduction in the bending stress as one layer of the laminated beam begins to dominate the differential expansion. When the two lamina have approximately equal bending stiffnesses—i.e., similar products of elastic modulus and cube of thickness—bowing and top-surface stress in the beam maximize.

This result shows that the “worst case” bimetallic strip effect can be avoided by selection of modulus and thickness values that produce a strong mismatch in the bending stiffnesses of the two layers. Figure 4-6b shows the effect of die attach thickness on the die surface stress. The laminated beam model predicts a reduction in stress as the thickness of the die attach is increased. Experimental data also included in the figure shows that the trends are similar although the effect saturates at higher attach thicknesses. This is probably due to time-dependent stress relaxation effects which are not taken into account in the model. Nevertheless, it is important to note that a die attach thickness of 0.001 to 0.002 in. is sufficient to reduce the stresses induced in the die attach process. This effect is also exhibited in the die attach region; a 2-D FEA model of attach shear stresses shows a similar thickness dependence (see Table 4-7).

Table 4-7. Effect of Die Attach Thickness on Bond Line Shear Stress Level

Die Attach Thickness (in.)	Shear Stress (psi/C)
0.000	102
0.001	33
0.002	33

Material property variations (elastic modulus, expansion coefficient) can produce significant changes in the die top-surface stress. On the one hand, selecting layer elastic moduli to give equal bending stiffnesses will maximize the top-surface stress for the reasons mentioned previously. On the other, when the expansion coefficients of the layers match, no differential expansion develops, and thermal stresses vanish.

Table 4-8 compares top-surface stresses for copper and Alloy 42 lead frame materials. As shown, with the Alloy 42 lead frame, the die level stress is $\sim 50\%$ of that for the copper lead frame. While the higher expansion coefficient of copper gives rise to higher process stresses at die attach, the effect is offset following encapsulation because copper and molding compound expansion coefficients are well matched. This effect is discussed later in this section.

Table 4-8. Effects of Lead Frame Material Properties on Die Stress Levels

Layer	Location	Stress (psi) Alloy 42 [†] Eutectic D/A*	Copper [†] Epoxy D/A [†]
Die	Top	+ 5750	+ 12200
	Bottom	- 11600	- 19500
Die Attach	Top	+ 33700	+ 33700
	Bottom	- 33100	- 33100
Lead Frame	Top	+ 6030	+ 12700
	Bottom	- 3940	- 2280

*Based on stress-free state of 363°C (eutectic temperature).

[†]Based on stress-free state of 135°C (epoxy D/A T_g).

NOTES:

1. Layer thicknesses: die, 0.015 in.; die attach, 0.001 in.; lead frame, 0.010 in.
2. Cooldown end point temperature: 20°C

The effect of die attach material properties on die stress has also been explored through both modeling and measurement. Tables 4-9 and 4-10 show experimental stress data from two separate tests for different adhesive die attach materials. This data indicates that top-surface stress can vary by almost an order of magnitude, depending on the adhesive selected (polyimide, epoxy, or thermoplastic). The greatest effect is found for materials with a low glass transition temperature.

Table 4-9. Experimental Values of Die Top-Surface Stress Components Following Die Attach

Die Attach Material	σ_{xx} (psi)	σ_{yy} (psi)	σ_{xy} (psi)	σ_{max} (psi)
Epoxy (Ablebond 84-1) 8 Samples	11600 ± 1020	10800 ± 1220	90 ± 604	12000 ± 1080
Polyimide (Ablebond 71-1) 19 Samples	26400 ± 13700	24200 ± 10000	-89 ± 1690	29300 ± 12300

Table 4-10. Effect of Different Die Attach Material Properties on Stress Level

Die Attach Material	Corner		Center	
	σ_{xx} (psi)	σ_{yy} (psi)	σ_{xx} (psi)	σ_{yy} (psi)
Thermoplastic (M & T)	3800 ± 2000	3300 ± 1900	3700 ± 2300	2200 ± 2000
Epoxy (Ablebond 84-1)	6700 ± 1700	4800 ± 1600	10300 ± 1300	9500 ± 1200
Polyimide (Ablebond 71-1)	40400 ± 7100	34400 ± 7000	45000 ± 12500	38300 ± 8500

Stresses in the package following molding have been calculated using the laminated beam analysis, and the results are displayed in Figures 4-7 through 4-9. As seen in Table 4-5, the difference in the expansion coefficient between the silicon and the molding compound is of the order of $15 (MC)^{-1}$. Qualitatively, this differential gives rise to post-cooldown stresses that are compressive in the die and tensile in the molding compound. Although the compressive stress may contribute to die reliability, the corresponding stress in the molding compound may lead to package cracking, particularly if the package is thin. Comparison of the actual stress with the fracture strengths given in Table 4-6 will enable the designer to determine the amount of margin available in a design.

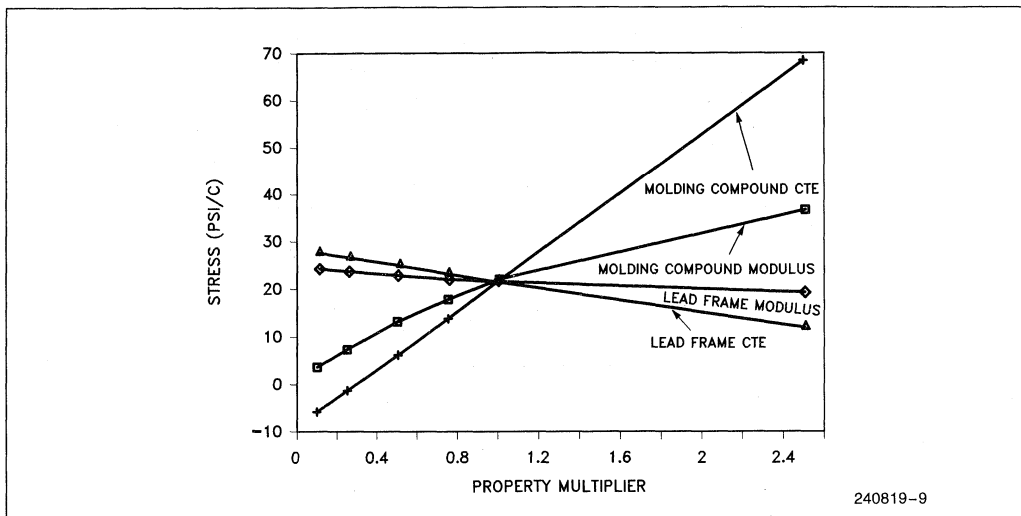


Figure 4-8. Variation of Plastic Stress above Die Surface with Molding Compound and Lead Frame Properties

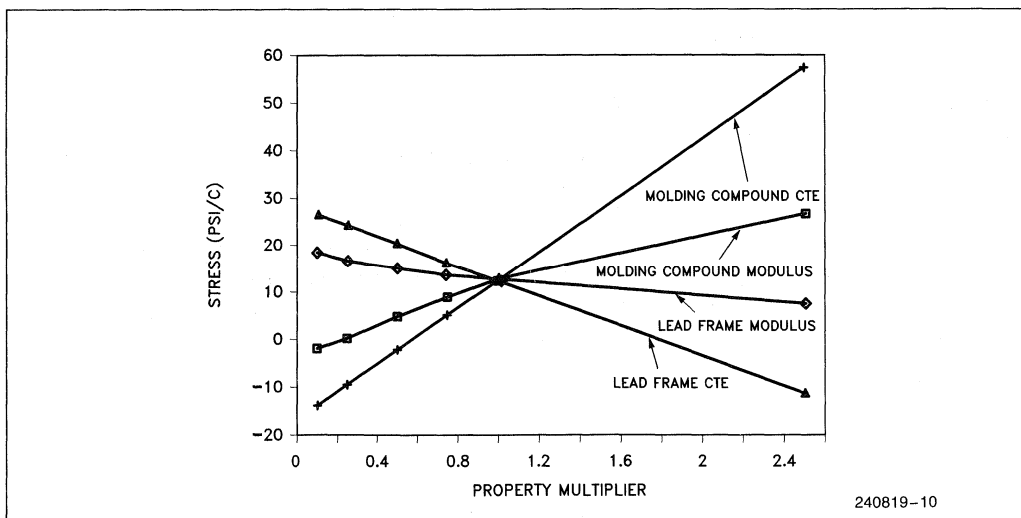


Figure 4-9. Variation of Plastic Stress below Die Paddle with Molding Compound and Lead Frame Properties

Package geometry effects on stress are illustrated in Figures 4-10 through 4-13, which include variations in package die, die attach, and lead frame thicknesses, as well as pad depress. The figures show that decreasing package thickness or increasing die thickness leads to reduced compressive stress on the die surface and increased tensile stress in the molding compound

adjacent to the die surface. Further, increasing die attach thickness has the same die-to-lead frame decoupling effect as decreasing its modulus or decreasing lead frame thickness. Compressive stresses at the top surface of the die can be increased, while tensile stresses in the adjacent molding compound can be reduced through pad depress (see Figure 4-13). However, tensile stresses in the compound adjacent to the die pad will increase, so a balance must be struck between top-side and bottom-side stresses in the molding compound. Use of these figures by package designers can lead to optimized product performance, since both device and package can be made reliable.

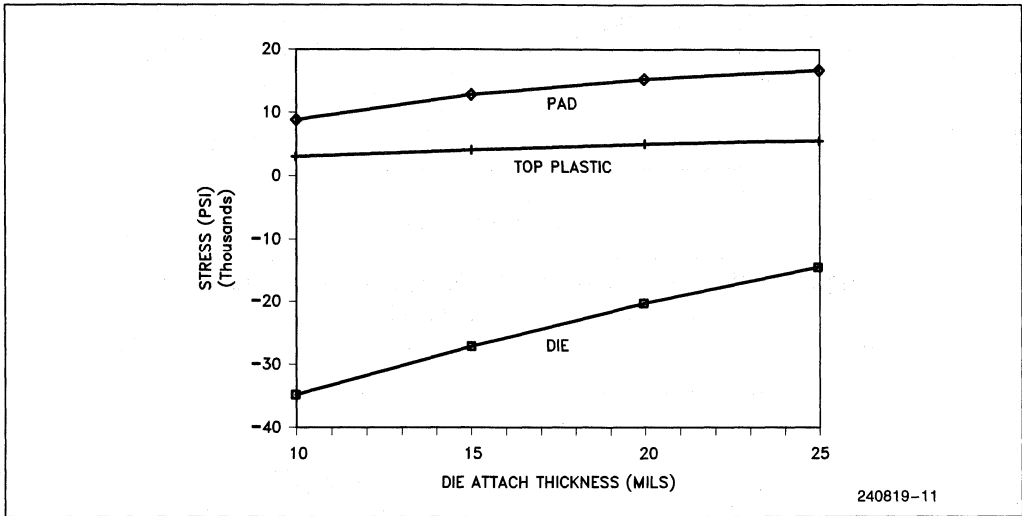


Figure 4-10. Variation of Plastic, Die and Pad Stress with Die Thickness

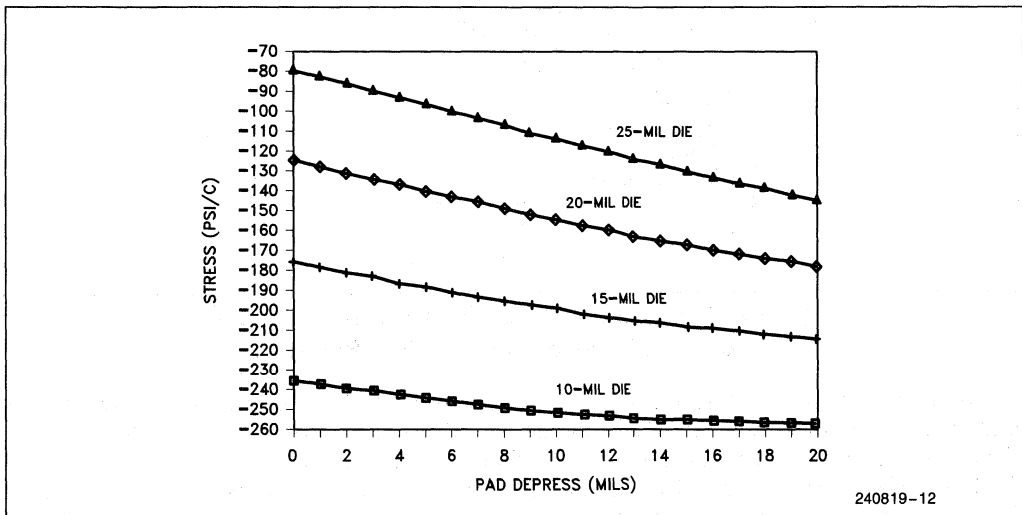


Figure 4-11. Variation of Die Stress with Pad Depress and Die Thickness

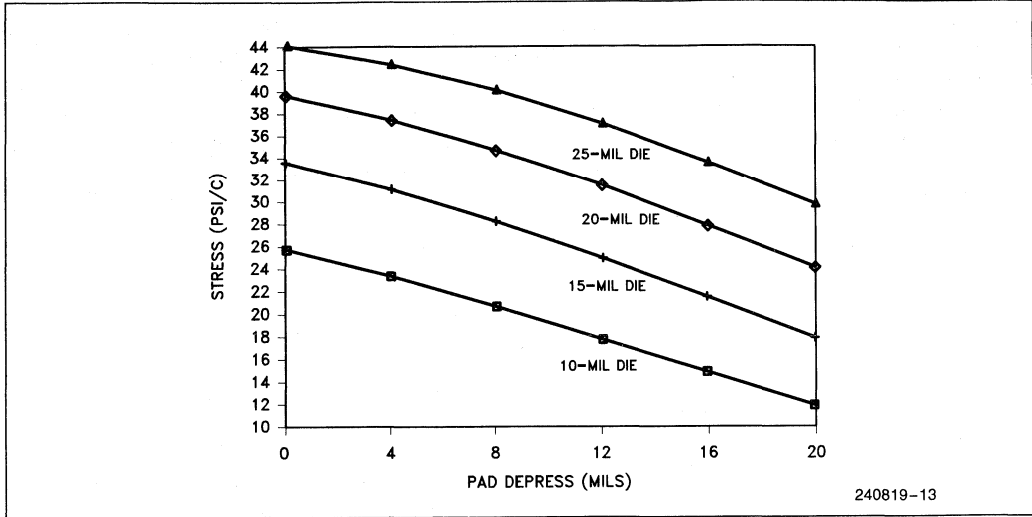


Figure 4-12. Variation of Plastic Stress above Die Surface with Pad Depress and Die Thickness

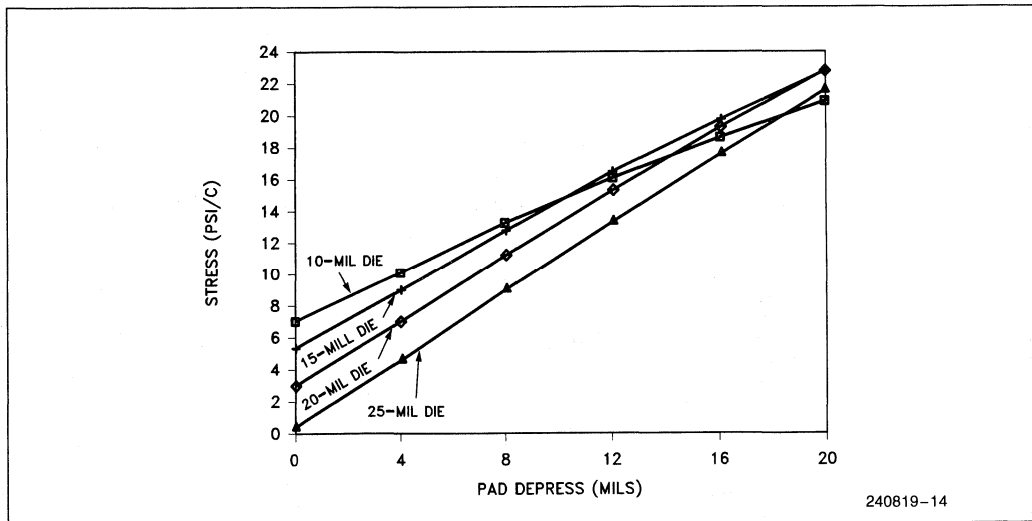


Figure 4-13. Variation of Plastic Stress below the Pad with Pad Depress and Die Thickness

Of continuing concern to design and process engineers is the effect of die size on the integrity and reliability of die attach. In fact, 2-D and 3-D FEA stress models confirm that once the die exceeds a critical size—usually about 10 times the die thickness (i.e., 0.200 in. for a die 0.20 in. thick)—stress magnitudes and distributions near the edge do not change. The reason for this seemingly anomalous result is that the characteristic length of the edge effect is governed by the thickness of the die or substrate (lead frame, plastic or ceramic base, etc.).

For the case of a die attached to a lead frame, the die thickness has the greatest effect. As shown in Figure 4-14, which illustrates the die attach shear stress distributions for die sizes varying from 0.190 to 0.390 in., the edge value is the same, although the distributions into the interior vary somewhat.

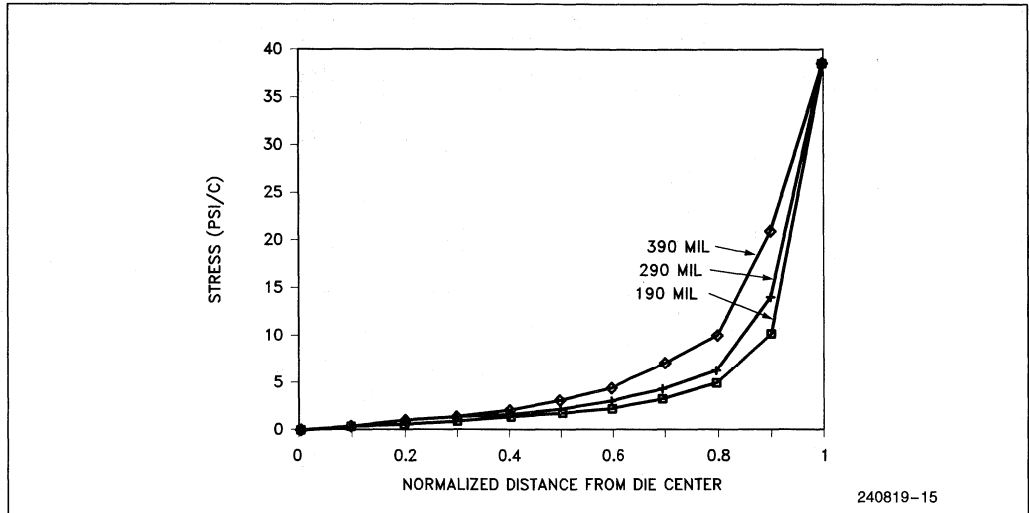


Figure 4-14. Shear Stress Distribution on Die Surface for Three Die Thicknesses

On an even larger scale, the 3-D FEA model of die attach shear stresses for the case of a 1.5-in. square die attached to an alumina substrate shows that the effect is limited to a border region approximately 0.300 in. in width (see Figures 4-15a and 4-15b). Again, the border dimension is governed by the die thickness (0.025 in.). In addition, formulas for bond stresses based on beam-on-elastic foundation analyses support the results obtained numerically (see Reference 2). Reports of die cracking and poor die attach reliability as the die size is increased beyond 0.500 in. suggest that the assumptions used in the model—i.e., constant thickness and material properties along the entire bond line—are not readily achieved in practice. Improvements in die backside preparation, in dispensing of the attach material, and in the drying and baking processes are generally required before the “small-die” performance levels can be reached.

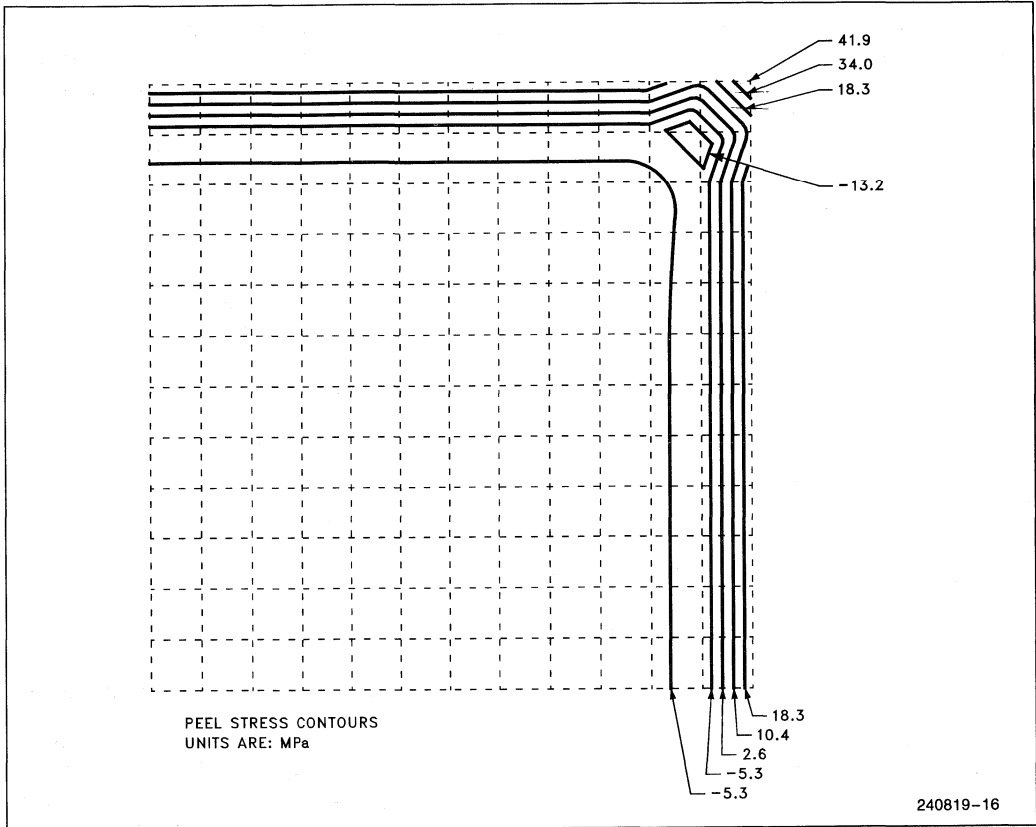


Figure 4-15a

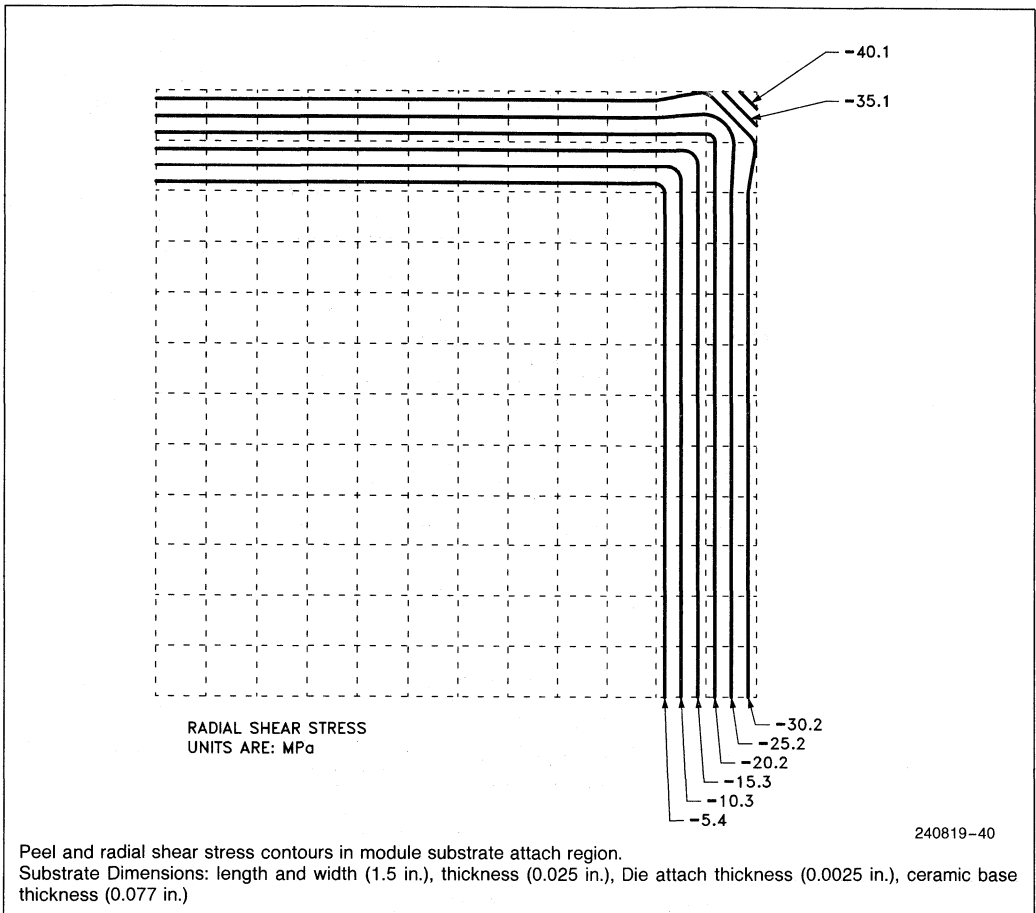


Figure 4-15b

INTERFACIAL STRESSES AND DELAMINATION

Numerous contributions have been made toward an understanding of the mechanisms associated with delamination of the encapsulant from the elements in the package (die, lead frame, etc.). Chief among these are the articles by Fukuzawa, et al. (see Reference 3), Belton et al. (Reference 4), Steiner and Suhl (Reference 5), and Bhattacharyya, et al. (Reference 6).

The key events or process steps leading up to delamination can be incorporated into a reasonably coherent picture on the basis of information presented in these references. Interfacial bonding occurs during cooldown from the mold and cure temperature, usually close to T_g , the glass transition temperature of the molding compound (see Figure 4-16a). Tensile stresses develop across the interfaces during heatup above T_g as part of the solder reflow process (see Figure 4-17a). Delamination sites initiate and grow under the proper set of environmental parameters, i.e., temperature, pressure, and sorbed moisture. Each of the process steps is reviewed in greater detail below to highlight the roles played by the important parameters during that step.

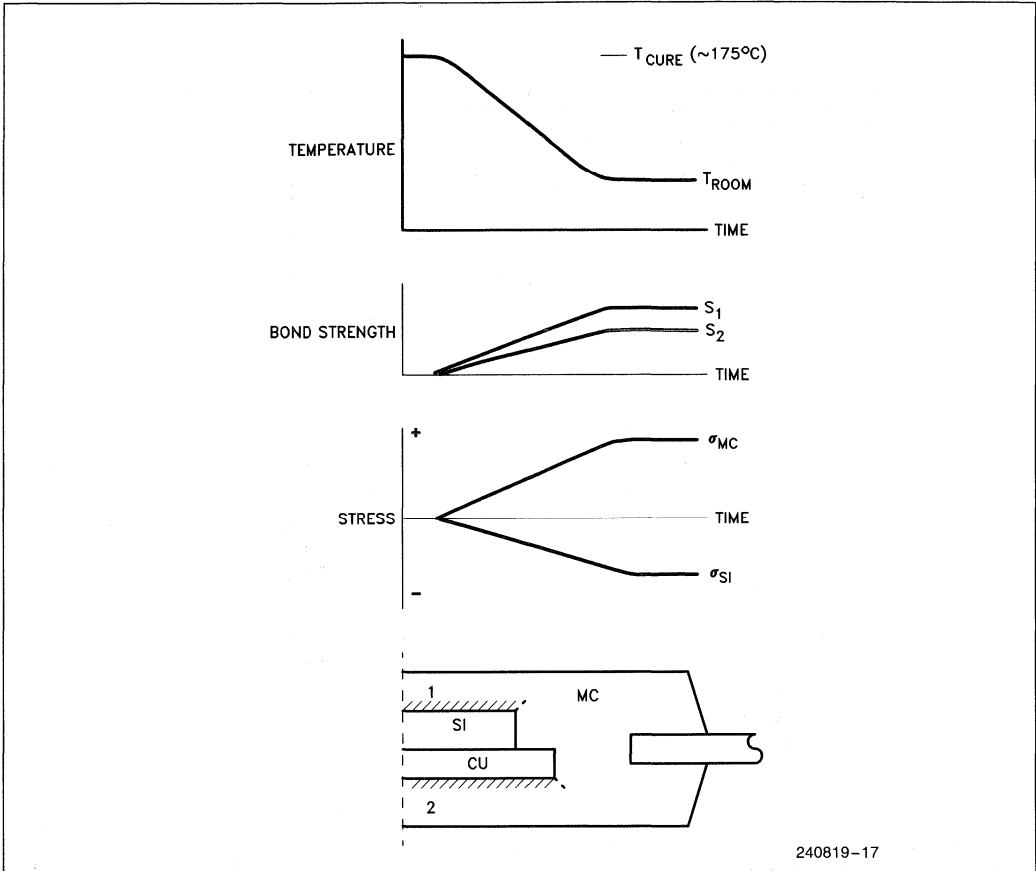


Figure 4-16. Cooldown Process

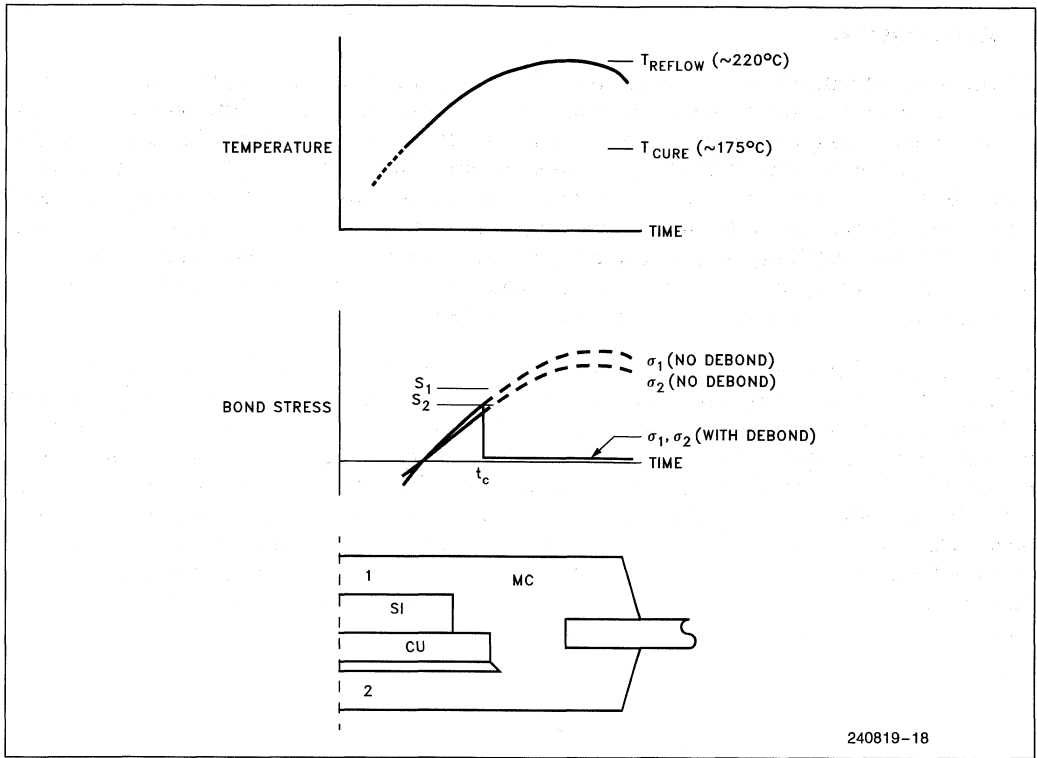


Figure 4-17. Reflow Process

Cooldown from T_g

In addition to bulk cross-linking, thermal stresses develop because of the differential thermal expansion (contraction) between the encapsulant and internal elements. As Figure 4-16c shows, this thermal stress field—tensile in the bulk encapsulant, compressive in the enclosed elements—is favorable to the development of a strong interfacial bond. The exact nature of the bond—chemical, mechanical, or other—is not fully understood. However, a favorable combination of temperature and time is expected to maximize the bond strength. Room temperature measurements indicate relatively strong bonds between encapsulant and silicon (> 1 Ksi) and somewhat weaker bonds between encapsulant and lead frame (see Figure 4-16b). Surface treatments (oxidation) and design features such as anchor wells and/or holes enhance the encapsulant/lead frame bond strength, although probably not above that of the encapsulant/silicon bond. Of particular interest in recent years is the influence of sorbed moisture on the bulk and interfacial properties of the encapsulant and internal elements. Measurements to date do not demonstrate any strong trends, although some interfacial bond strength degradation is suggested.

Heatup above T_g

As the package temperature is raised above T_g during the solder reflow process, the thermal stress state passes through its neutral point and then reverses sign; i.e., the bulk encapsulant stress becomes compressive, the internal elements tensile. The interfacial bond is placed in tension, and delamination will occur first at sites where the bond strength is exceeded. Other things being equal, an isotropic stress state will initiate delamination at the encapsulant/lead frame interface because of its intrinsically lower inherent strength (see Figure 4-17b). Delamination stability/instability will depend on the stress state and the intrinsic fracture resistance of the bond; indeed, some analogy may be made to crack initiation and propagation in a homogeneous material with known fracture toughness.

The presence of moisture can complicate the delamination process significantly, adversely affecting mechanical properties such as modulus and thermal expansion coefficient, and reducing interfacial bond strength. In addition, the moisture trapped at and near the interfaces may be in the liquid phase at the start of the heatup cycle and be driven to saturation pressure levels associated with reflow temperatures (> 300 psi; see Figure 4-18b), since there is insufficient time for moisture release outside the package. According to numerous independent measurements, bulk diffusivity decreases with moisture concentration. As a result, moisture discharge occurs more slowly than moisture uptake, and the reflow temperature profiles do not allow adequate time to prevent or reduce saturation pressure build-up.

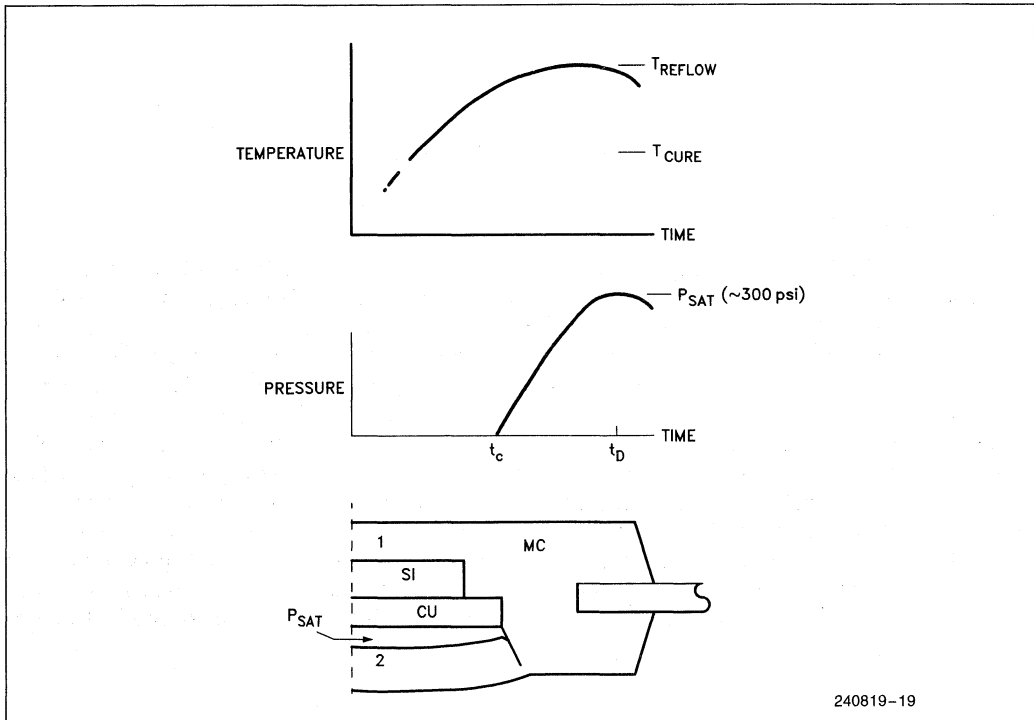


Figure 4-18. Pressure Buildup during Reflow

As discussed in References 3 and 6, the size and shape of the package and its contents play an important role in the integrity and reliability of the interfacial bonds. When the package is thin, and the die and die paddle both large, there is the potential for the development of high tensile stress in the bulk encapsulant adjacent to the bottom corner of the die paddle or at the top corner of the die during the reflow process. This stress results primarily from the delamination caused by the heatup-induced interfacial tensile stresses in combination with the saturation pressure build-up at the interface when sufficient moisture is trapped in the encapsulant to act as a source of high-pressure water.

As shown in References 3 and 6, the governing geometric parameter is L/h , the ratio of the die or die paddle size to the thickness of the package beneath the paddle or above the die. This parameter serves as a multiplier of the saturation pressure for estimating the stresses in the encapsulant at the critical corner zone. Theoretical considerations suggest that the encapsulant should not fracture as long as $L/h < 6$; above this level, the encapsulant fractures, and a crack propagates from the corner outward to the free surface of the package. Data compilation (see References 7 and 8) suggests that $L/h < 5$, although the linear relation between L and h is confirmed. Under extreme conditions, the failure is accompanied by a snapping sound and has been dubbed the “popcorn effect”. Bulging of the package surface above the delaminated zone (see Figure 4-18c) reinforces this analogy. An adequate supply of high-pressure water is necessary to support the bulging. Moisture weight gains of 0.1%, said to be the critical level for the popcorn effect, are more than adequate for bulge heights of 0.001 in. in a 0.200-in. delamination zone. Not only is the bulge cosmetically unacceptable, but it is generally accompanied by cracks from the die/die paddle edge to the outside of the package.

Selection of material properties, control of the environment, and careful design can reduce, if not prevent, delamination and associated failure mechanisms in the package. Increasing delamination strength is of prime importance and can be achieved through both mechanical and chemical means. Since die-paddle cracking is most prominent, treatment of the metallic surface—oxidizing, roughening, or designing of anchor well or through-holes—is receiving considerable attention. Results are still preliminary but are encouraging. Modification of material properties to achieve higher encapsulant fracture strength and to reduce moisture uptake is ongoing, although major breakthroughs have not been reported or expected. There is little enthusiasm in the systems design arena to raise the package profile; indeed, there is pressure to reduce package thickness (i.e., h) even further. As a result, it will be important to limit die and paddle sizes as much as possible. Even this objective is thwarted by device designers who seek to add more functionality to their product, leading to an increase in device size (i.e., L).

Because of the key role played by trapped moisture in the internal pressurization effect, keeping the weight gain below 0.1% is critical. This is achieved through the “bake and bag” process before product shipment. Desiccated barrier bags have been shown to provide at least six months’ protection against critical moisture build-up in the package. Parts used beyond the storage life can be rebaked prior to reflow to recover safe moisture levels. Until the enhancements discussed earlier can be accomplished, the bake and bag steps will be an important part of the process for reliable board-level assembly.

Bond Stresses

In addition to the mechanical and metallurgical stresses developed during the wire-bonding process, encapsulation and environmental stresses subsequent to bonding can contribute to degradation of the interconnection. Reliable first and second bonds can be ensured by bonding within the process windows for force, power, time, and temperature. Excursions beyond these windows are minimized through regular process monitors such as bond pulls. Both pull strength and failure mechanism criteria must meet specifications. In particular, no cratering failures are acceptable even if pull strength criteria are met, since craters indicate excessive force during bonding, which could lead to reliability problems in the field.

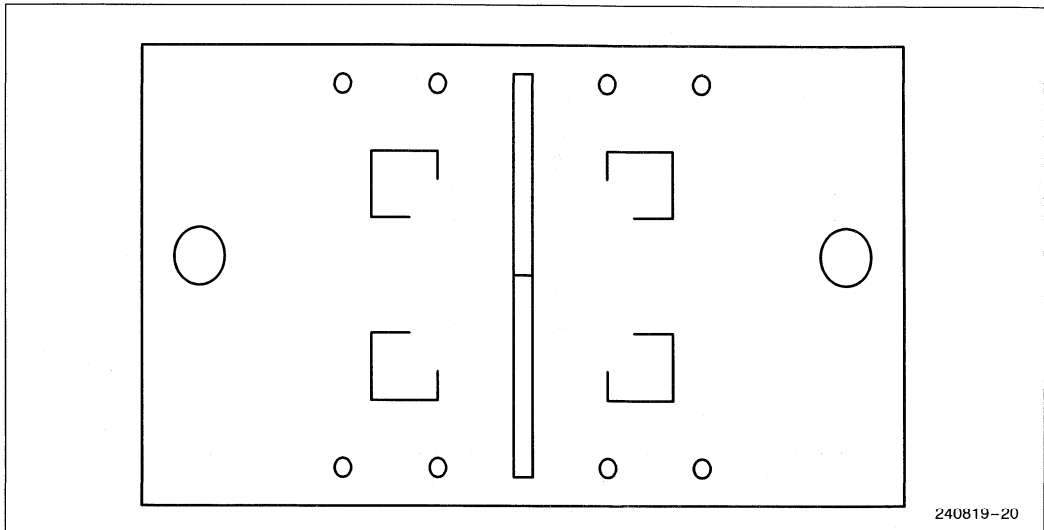
During encapsulation, wire sweep may occur if wire lengths are too great or if drag during molding flow is excessive. Current mold gate designs provide low drag flow patterns, and X-ray monitors are used to confirm process stability. Wire diameter and length design rules are strictly enforced to ensure that there is adequate mechanical stability of the bond arch to resist the drag forces. Development of new package designs includes analysis and experiment to ensure that wire sweep is minimized.

In plastic packages, delamination at the interface between the molding compound and silicon or lead frame can cause high stresses at the first or second bond location, because the differential thermal expansions must be accommodated across the bond itself. The delamination generally results from temperature cycling of packages with trapped moisture. To suppress the adverse effects of delamination, selection of materials with enhanced interfacial adhesion and the design of lead frames that feature additional mold compound locking characteristics have proven to be effective. Three-dimensional FEA models are used to guide and optimize the designs. For packages that are particularly moisture-sensitive, shipment of prebaked product in sealed moisture-proof bags with desiccant ensures that delamination is minimized and operation of the assembled part will be reliable.

Compliant Leads and Solder Joint Fatigue

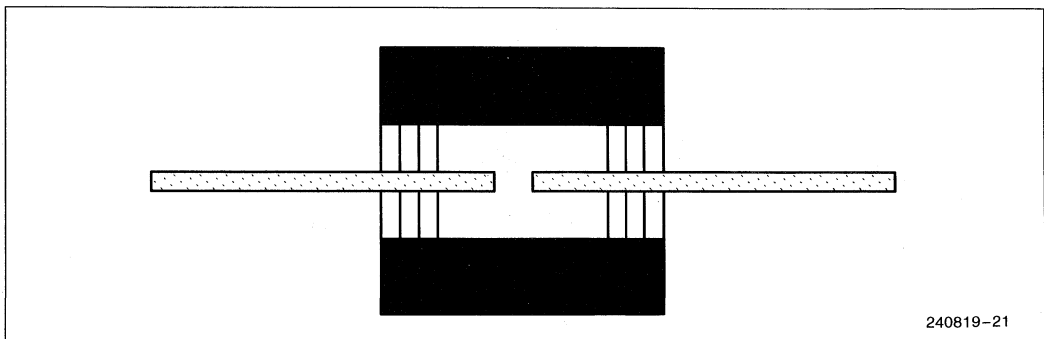
With the advent of surface mounted packages, solder joint integrity became an issue of considerable concern. It was found that solder joints on leadless ceramic packages measuring more than 0.5 in. on a side could survive only a few hundred temperature cycles (Condition B, -55°C to $+125^{\circ}\text{C}$) when the packages were surface mounted to FR4-type circuit boards. The addition of compliant leads to these packages has extended the life considerably and is now used in the design of all new surface mounted packages.

As a means of experimentally evaluating the in situ stiffnesses of leads on packages surface-mounted to boards, the straddle board method has proved to be a very useful tool (see Reference 2). As shown in Figures 4-19 and 4-20, the straddle board consists of a slotted, double-sided epoxy-glass FR-4 board that is patterned for corner leads; all other package leads are removed.



240819-20

Figure 4-19. Lead Stiffness Straddle Board



240819-21

Figure 4-20. Straddle Board with Two Packages in Place

Units are mounted on both sides of the board using production-level processes and specifications for each package. The board is mounted vertically in a tensile test set-up such as a materials test system (MTS), and the narrow sides of the slot are cut, separating the two ends of the package. The MTS is fitted with a 200-lb. load cell and a 6-in. displacement actuator. This allows the straddle board to be tested with a 0.020-in. displacement, 0.010 in. in the tensile cycle and 0.010 in. in the compressive cycle. These values were chosen to span the lead displacement experienced during temperature excursions from -65°C to $+150^{\circ}\text{C}$ (MIL-STD-883C T/C [C]).

A total cycle time of five seconds was used with a maximum load range of 0.8-8 lb., depending on the package type and lead count. As Figure 4-21 shows, leads are loaded in both lateral and transverse directions (i.e.; in the plane and normal to the plane of the lead bend). Twenty-five samples per lead count per direction were evaluated. Once the board was mounted, three full cycles were run, and the force vs. deflection curve was recorded. The linear portions of the loading and unloading curves were used to determine the lead stiffness. A typical hysteresis curve is shown in Figure 4-22.

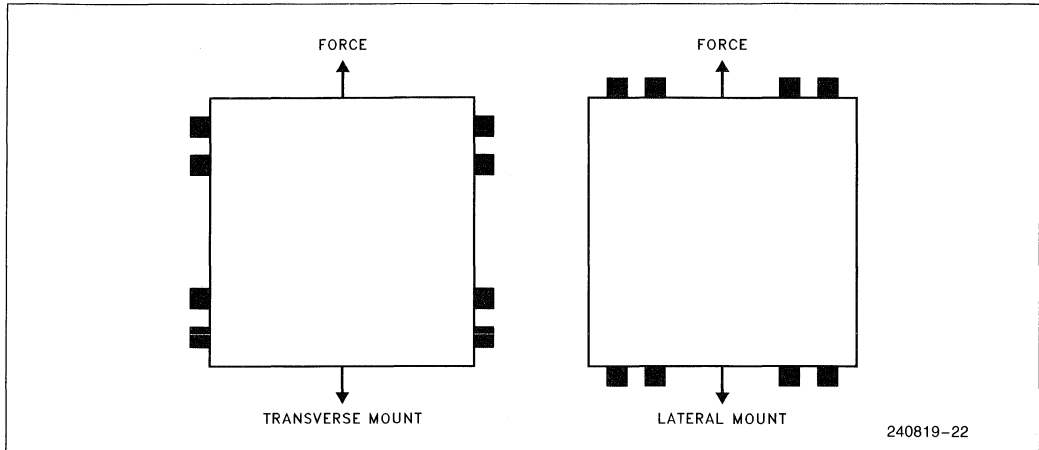


Figure 4-21. Orientation of Applied Load

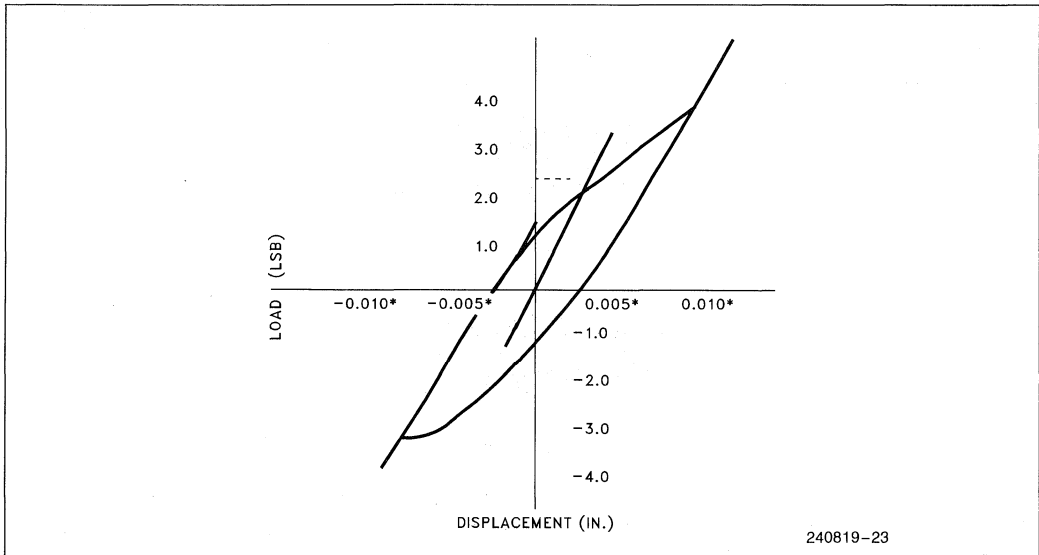


Figure 4-22. Lead Stiffness Determined from Hysteresis Curve

Designing leads with adequate compliance is now recognized as an important element of overall product design, and mechanical modeling has proved to be a useful design tool. Lateral and transverse lead stiffnesses were calculated for PLCC, cerquad, and PQFP packages using the ANSYS 3-D elastic beam element option (see Reference 4). The calculated stiffness for each type of package was matched to the value obtained from the straddle board measurements by locating the point on the lead where agreement was reached. In all cases, the point lay within the solder joint, in agreement with physical expectations.

Of particular interest were the boundary conditions imposed by the solder joint on the foot of the lead. In the lateral direction, the solder volume is adequate for the joint to provide built-in support to the lead foot (zero rotation). However, in the transverse direction for the PLCC and cerquad packages, the J-bend lead stiffnesses are large enough to produce inelastic deformations in the solder joint. As a result, the joint acts like a pinned support (free rotation). In all cases, the PQFP gull-wing leads are sufficiently compliant for the solder joint to act as a built-in support. This result suggests that reducing lead stiffness will significantly reduce solder joint stresses and associated creep and fatigue. Experimental data recently reported in Reference 3 supports this hypothesis.

Experience to date indicates that in situ lead stiffnesses below 100 lb./in. give satisfactory compliance (see References 1 and 4). Gull-wing leads on 0.025-in. pitch (PQFP and CQFP) fall into this category. Details of the use of straddle boards for the measurement of lead stiffnesses, both in the plane and normal to the plane of the lead bend, are given in Reference 5. Modeling of the lead stiffness using the 3-D beam element option in the ANSYS software is described in Reference 4. Representative in situ stiffnesses for PLCCs, cerquads, and PQFPs are shown in Table 4-11.

Table 4-11. Summary of Lateral and Transverse Lead Stiffness Matching Points for Various Lead Geometries

Package Type	S1 (lb./in.)	Y1 (in.)	St (lb./in.)	Yt (in.)
44-Lead PLCC	323.0	0.0065	440.0	0.0055
68-Lead PLCC	187.0	0.0100	330.0	0.0045
44-Lead CERQ	130.0	0.0120	374.0	0.0045
68-Lead CERQ	119.0	0.0090	308.0	0.0035
100-Lead PQFP	40.0	0.0090	38.0	0.0035



IC PACKAGE THERMAL CHARACTERISTICS

Importance of Thermal Management

Thermal management of an electronic system encompasses all the thermal processes and technologies that must be utilized to remove and transport heat from individual components to the system thermal sink in a controlled manner.

Thermal management has two primary objectives. The first is to ensure that the temperatures of all components are maintained within both their functional and maximum allowable limits. Functional temperature limits provide the temperature range within which the electrical circuits may be expected to meet their specified performance requirements. Operation outside this range may result in degraded machine performance or logic errors. The maximum allowable temperature limit is the highest temperature to which a component or part of a component may be safely exposed. Operation above the maximum allowable temperature limit may result in actual physical destruction of the component or irreversible changes in its operating characteristics.

The second objective of thermal management is to ensure that distribution of component operating temperatures satisfies reliability objectives. Although failure to meet this objective may not be as readily apparent as failing to remain within maximum temperature limits, in the long run it can be equally costly. Failure mechanisms encountered in electronic components are kinetic in nature and depend exponentially on device operating temperature. The exact relationship between failure rate and temperature depends upon the packaging materials and processes, and the failure mechanism in operation. This relationship can be illustrated for changes in device characteristics resulting from chemical or diffusive processes by using a normalized failure rate defined by an Arrhenius equation:

$$\theta_n = \frac{\theta_T}{\theta_{Tr}} = \text{Exp} [(E_A/k) (T_R^{-1} - T^{-1})] \tag{1}$$

where:

- θ = Failure rate
- θ_n = Normalized failure rate
- T = Absolute junction temperature (K)
- Tr = Reference temperature (K)
- EA = Activation energy (eV)
- k = Boltzmann's constant: 8.616×10^{-5} (eV/K)

Equation 1 is plotted for a reference temperature of 100°C and activation energies of 0.4 eV to 1.0 eV in Figure 4-23. According to this figure, a 25°C increase in operating temperature above the reference temperature results in approximately a five- to six-fold increase in failure rate with activation energy of 0.6 eV to 0.8 eV. Thus, tight control of package temperature is essential to product reliability.

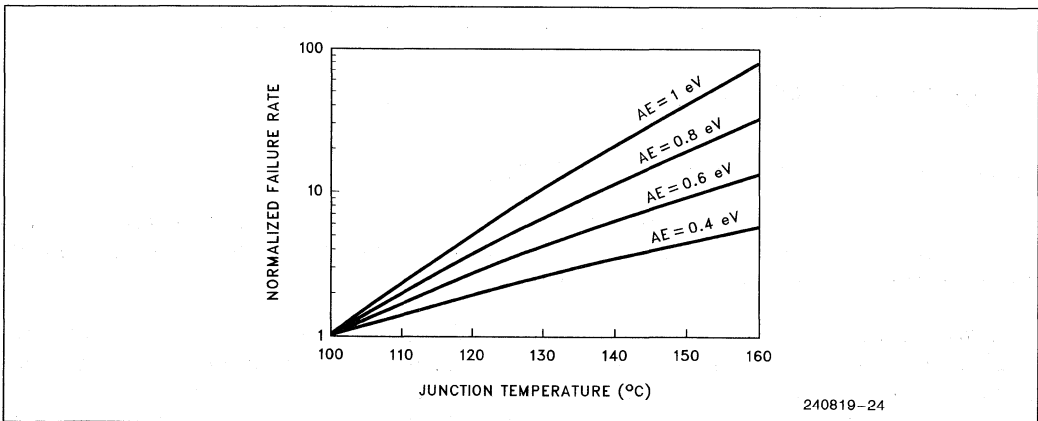


Figure 4-23. Component Failure Rate as a Function of Junction Temperature

Thermal Impedance

The junction-to-ambient and junction-to-case thermal resistance values are used as measures of IC package thermal performance. These parameters are defined by the following relations:

$$\theta_{ja} = \frac{T_j - T_A}{P} \quad (2)$$

$$\theta_{jc} = \frac{T_j - T_C}{P} \quad (3)$$

$$\theta_{ja} = \theta_{jc} + \theta_{ca} \quad (4)$$

where:

θ_{ja} = Junction-to-ambient thermal resistance (C/W)

θ_{jc} = Junction-to-case thermal resistance (C/W)

θ_{ca} = Case-to-ambient thermal resistance (C/W)

T_j = Average die temperature (C)

T_c = Case temperature at a predefined location (C)

P = Device power dissipation (W)

T_A = Ambient temperature

θ_{jc} is a measure of package internal thermal resistance from silicon die to package exterior. This value is strongly dependent upon packaging material, thermal conductivities, and package geometry. On the other hand, θ_{ja} values include not only package internal thermal resistance, but also the conductive and convective thermal resistance from package exterior to the ambient. θ_{ja} values depend on material thermal conductivities and package geometry as well as ambient conditions such as flow rates and coolant physical properties.

To guarantee component functionality and long-term reliability, the maximum device operating temperature is bounded by setting constraints on either ambient temperature or package exterior temperature at predefined locations. Ambient temperature is most often measured at an undisturbed location at a certain distance away from the package. As defined in Intel experiments, the case temperature is measured at the center of the package's top surface. Depending on the ambient and board temperatures in the systems environment, thermal enhancements such as heat fins or forced air cooling may be necessary to meet the case or ambient temperature requirements.

Test Methodology

To calculate thermal resistance values, junction temperature is measured using the temperature-sensitive parameter (TSP) method. This method uses special test structures cut to the same size as the actual device, consisting of resistors and diodes. Resistors are used to simulate the device power dissipation and thus heat up the package. Diodes located at different points on the chip surface are used to measure the temperature.

A single package is mounted either directly or via a socket to a thermal test board, which is oriented vertically in the test chamber. Two different test board designs are used for surface mount and through-hole mount packages, as shown in Figure 4-24. The test chamber volume

is 1 ft.³, and the ambient temperature is measured 12 in. away from the package (see Figure 4-25). Initially, the diodes are forward-biased to a 100 μ A constant current source, and the test board assembly is immersed in a constant temperature dielectric fluid bath. By changing the bath temperature, diode voltage output is calibrated vs. bath temperature.

Next, the test structure is powered up, and diode voltage drop is monitored until no change is detected in the voltage level, indicating an equilibrium state. At this stage, the diode voltage drop, ambient and case temperatures, and device voltage drop and current are recorded. Case temperature is measured at the center of the package's top surface by means of a thermocouple attached with thermally conductive paste to minimize contact thermal resistance. If a heat fin is mounted on the package, case temperature is measured at the center of the heat fin base (see Figure 4-26). In moving-air thermal resistance measurements, the test board assembly is exposed to a uniform velocity laminar air flow. In this case, air velocity is measured upstream 12 in. away from the board's leading edge, using a hot wire anemometer. Air temperature is also measured at the same point.

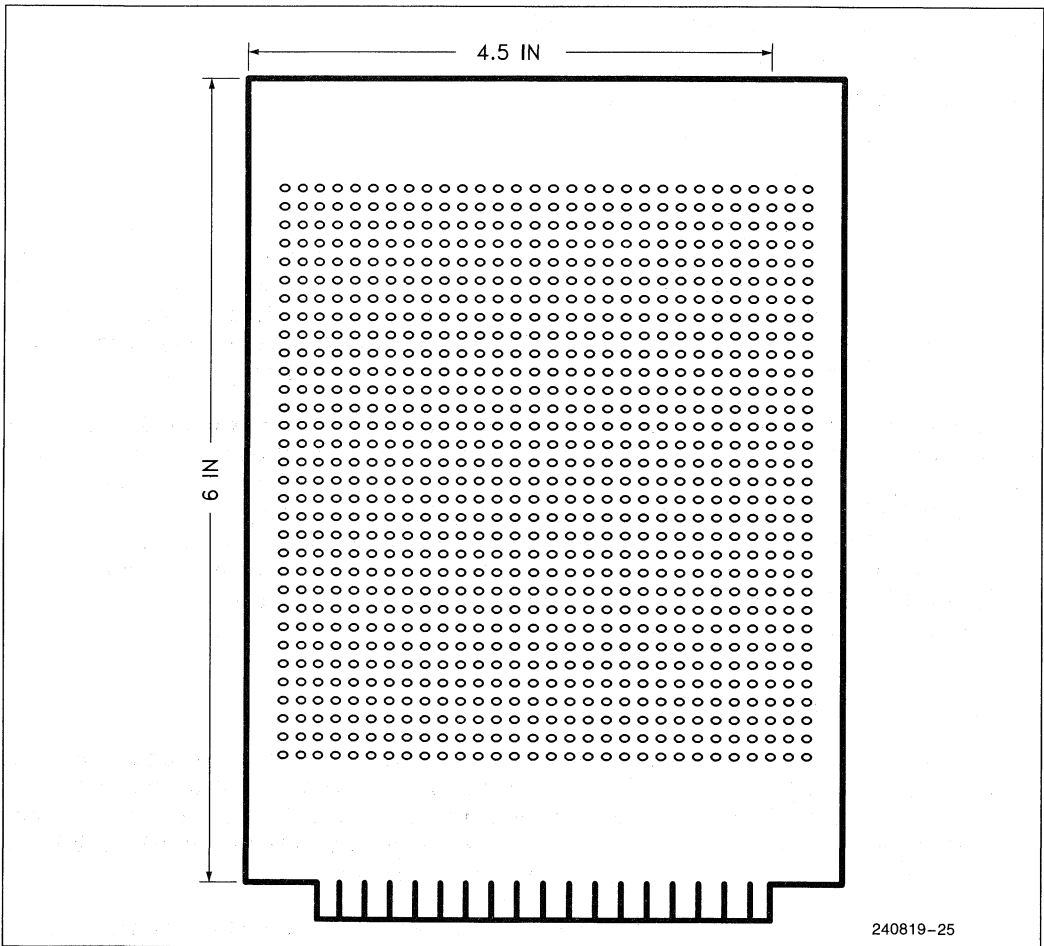
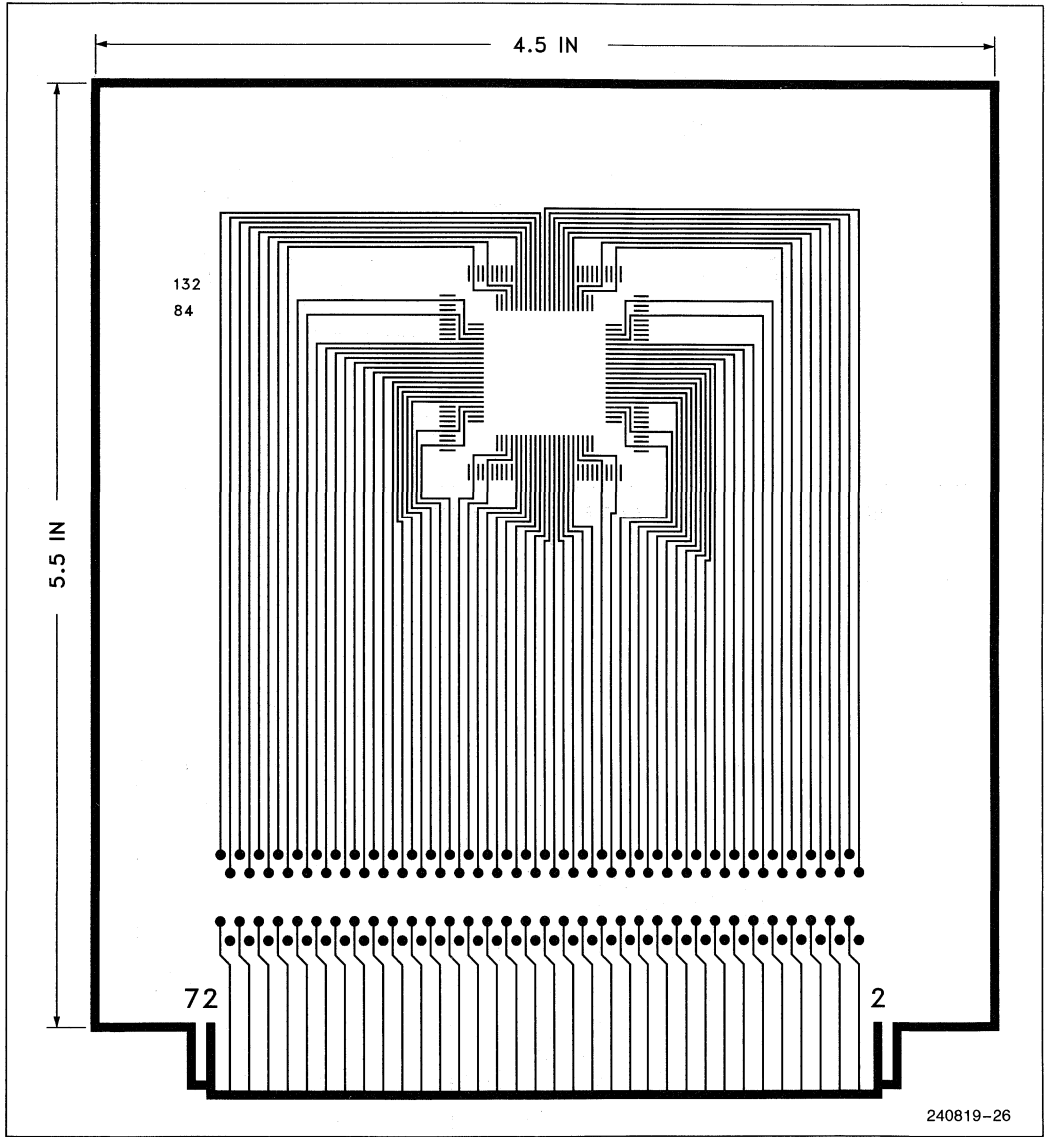


Figure 4-24a. Thermal Test Board for Through Hole Mount Component



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Figure 4-24b. Thermal Test Board for Surface Mount Component

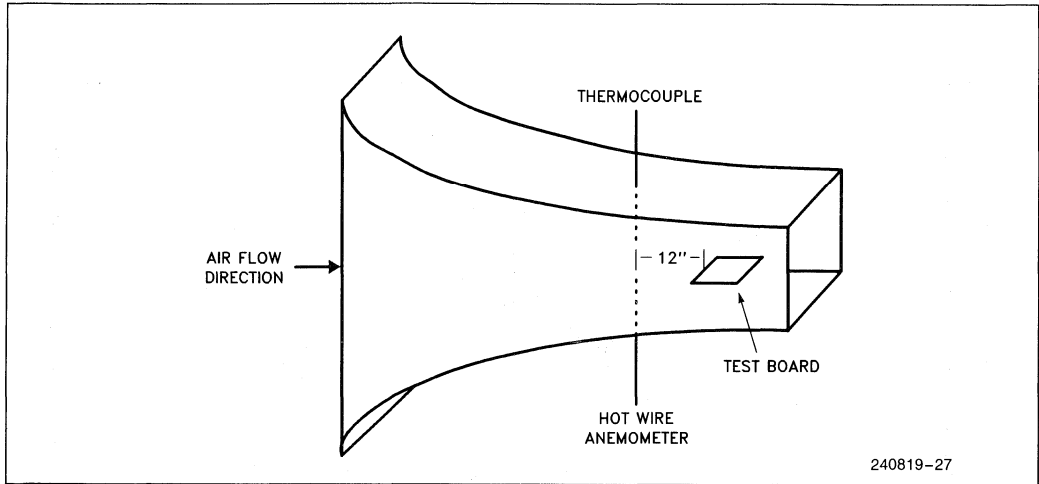


Figure 4-25. Test Chamber for Thermal Performance Testing

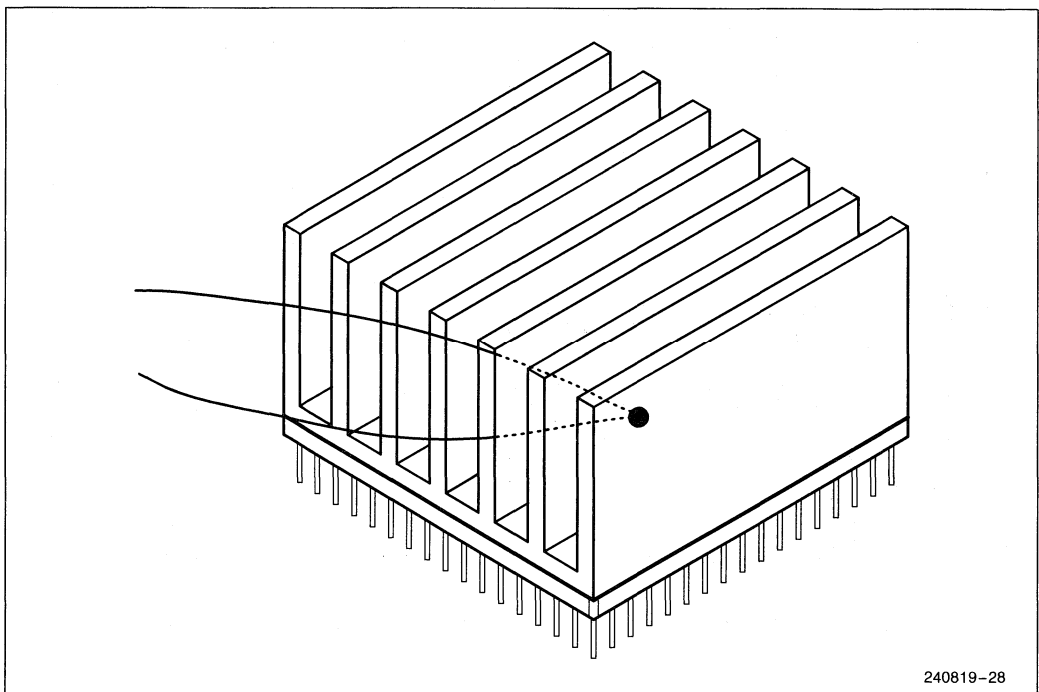


Figure 4-26. Location of Package Case Temperature Measurement

Heat Transfer Modes

To understand the thermal characteristics of ICs, it is necessary to briefly review the processes by which heat is transferred from one point to another. There are three heat transfer modes: conduction, convection, and radiation.

CONDUCTION

Conduction is a process by which heat flows from a region of higher temperature to one of lower temperature within a medium (solid, liquid, or gaseous) or mediums in direct physical contact. In conductive heat flow, the energy is transmitted by direct molecular communication without appreciable displacement of the molecules.

In a one-dimensional system (see Figure 4-27), conductive heat transfer is governed by the following relation:

$$q = -kA \frac{\Delta T}{L} \tag{5}$$

where:

q = Heat flow rate (W)

k = Material thermal conductivity (W/C M)

A = Cross-sectional area

$\frac{\Delta T}{L}$ = Temperature gradient (C/M)

Equation 5 indicates that in conduction, the heat flow rate is directly proportional to material thermal conductivity, temperature gradient, and cross-sectional area. Equation 5 can be written as:

$$q = \frac{\Delta T}{L/kA} \tag{6}$$

Using an electrical analogy, if q and ΔT are analogous to current and voltage respectively, L/kA will be analogous to thermal resistance. According to Equation 6, thermal resistance can be expressed in terms of material thermal conductivity and geometrical parameters.

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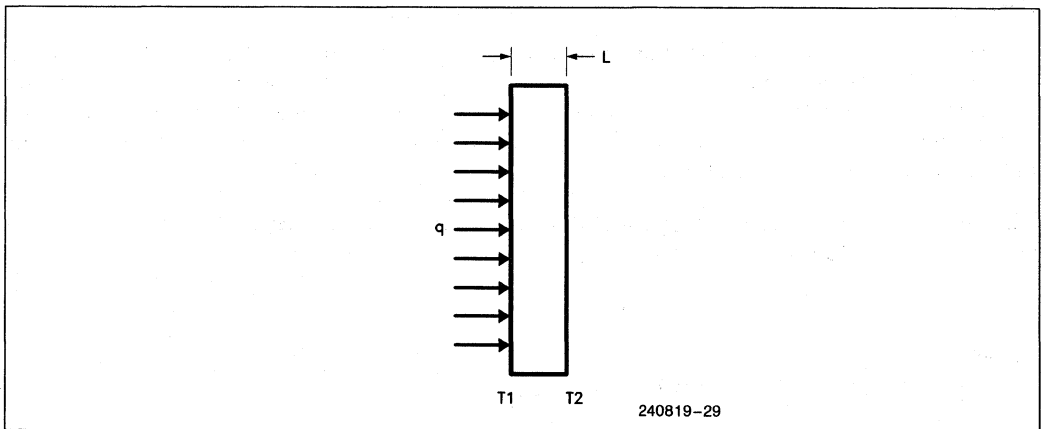


Figure 4-27. One-Dimensional Heat Flow by Conduction

CONVECTION

Convection is a process of energy transport by the combined action of heat conduction, energy storage, and mixing motion. Convection is most important as the mechanism of energy transfer between a solid surface and a fluid. The basic relation that describes heat transfer by convection from a surface presumes a linear dependence on surface temperature rise, and is referred to as Newtonian cooling:

$$q_c = h_c A (T_s - T_a) \quad (7)$$

where:

q_c = Convective heat flow rate from a surface to ambient (W)

A = Surface area (M^2)

T_s = Surface temperature (C)

T_a = Ambient temperature (C)

h_c = Average convective heat transfer coefficient (W/M^2C)

Equation 7 can also be written as:

$$q_c = \frac{T_s - T_a}{1/h_c A} \quad (8)$$

which shows that convective thermal resistance is defined as $1/h_c A$.

In forced convection, fluid flow is caused by an external factor such as a fan, while in free or natural convection, fluid motion is induced by density differences resulting from temperature gradients in the fluid. Under the influence of gravity or other body forces, these density differences give rise to buoyancy forces that circulate the affected fluid and convect heat toward or away from surfaces wetted by the fluid.

RADIATION

Thermal radiation is defined as radiant energy emitted by a medium by virtue of its temperature, without the aid of any intervening medium. The physical mechanism of radiation is not yet completely understood. Radiant energy is sometimes envisioned to be transported by electromagnetic waves, at other times by photons. Neither viewpoint completely describes the nature of all observed phenomena.

The amount of heat transferred by radiation between two bodies at temperatures T_1 and T_2 is governed by the following expression:

$$q = \epsilon \sigma A (T_1^4 - T_2^4) \quad (9)$$

where:

q = Amount of heat transferred by radiation (W)

ϵ = Emissivity $0 < \epsilon < 1$

σ = Stefan-Boltzmann constant, 2.36×10^{-11} ($W/M^2 K^4$)

A = Area (M²)

F₁₂ = Shape factor between surfaces 1 and 2 (A fraction of surface 1 radiation seen by surface 2)

T₁, T₂ = Surface temperatures (K)

For radiation to make a rather significant contribution compared to either natural convection or forced convection mechanisms, a relatively large temperature difference must exist between T₁ and T₂. In the case of most low-power electronic applications, these temperature differences are relatively small, and therefore, radiation effects are normally neglected. But for power applications, heat transfer by radiation should be considered. To compare radiative and convective effects, a radiation heat transfer coefficient is defined as:

$$h_r = \epsilon \sigma F_{12} (T_1^2 + T_2^2) (T_1 + T_2) \tag{10}$$

where h_r is the radiative heat transfer coefficient.

Factors Impacting Package Thermal Resistance

The thermal resistance of a package is not a constant entity. There are several packaging and environmental parameters as well as mounting configurations that impact thermal resistance values. The following is a summary of those parameters.

PACKAGE SIZE

As shown by the one-dimensional conductive and convective thermal resistance expressions (see Equations 6 and 8), thermal resistance is inversely proportional to area. This means that as the packages get larger, thermal resistance becomes smaller due to an increase in the heat transfer area. Figure 4-28 shows typical junction-to-ambient thermal resistance values as a function of lead count for different package families. According to this figure, thermal resistance is lower for higher lead counts (larger package size) of the same package family.

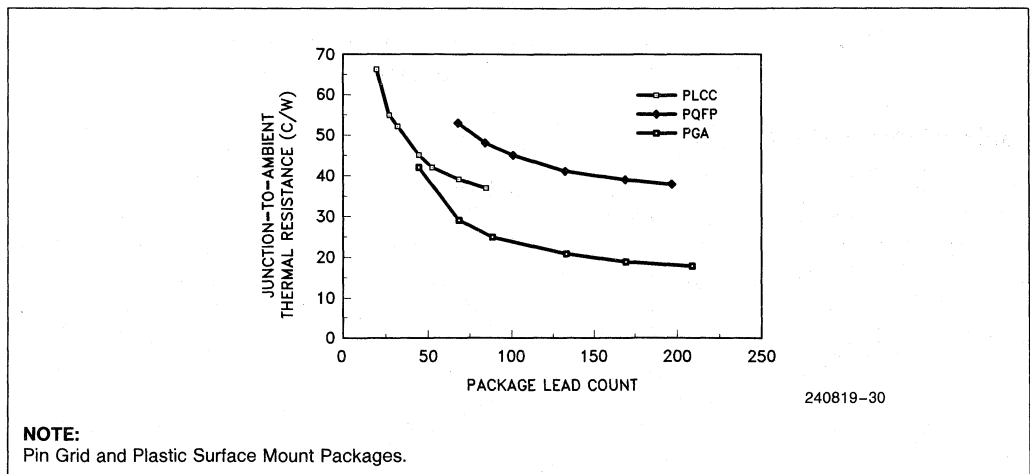


Figure 28a. Effect of Package Size on Thermal Resistance of PLCC, PQFP, and PGA Packages

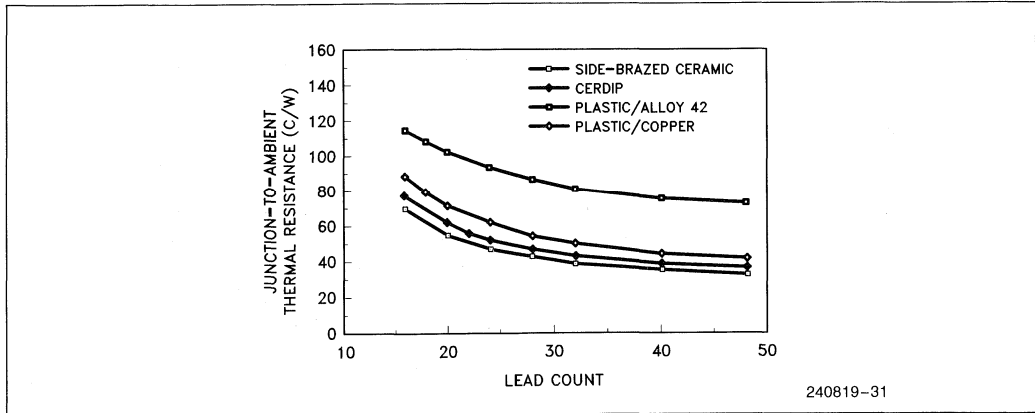


Figure 4-28b. Effect of Package Size on Thermal Resistance of Plastic and Ceramic Dual-In-Line Packages

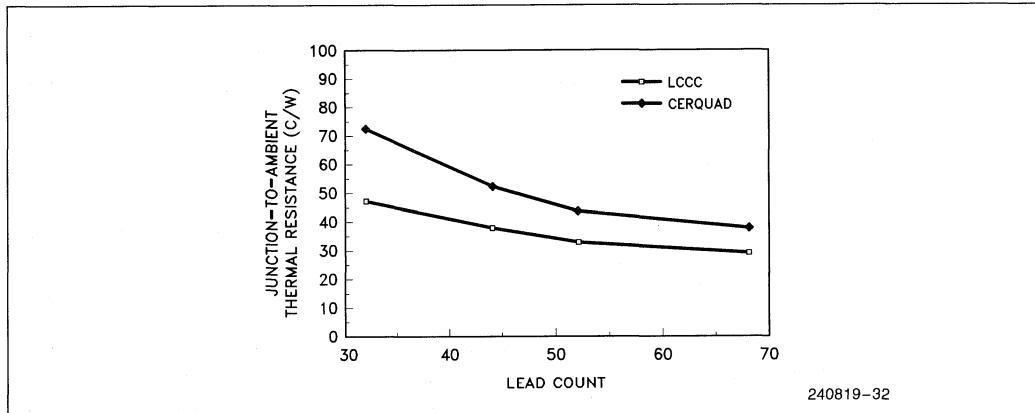


Figure 4-28c. Effect of Package Size on Thermal Resistance of CerQuad and Leadless Ceramic Chip Carriers

PACKAGING MATERIAL THERMAL CONDUCTIVITY

Again, the one-dimensional conductive thermal resistance expression shows that thermal resistance is inversely proportional to the thermal conductivity of the packaging material. For example, aluminum oxide, the most commonly used ceramic material, has a thermal conductivity that is an order of magnitude larger than plastic materials. As a result, the internal resistance of ceramic packages is substantially lower than the plastic packages from the same family, resulting in lower overall thermal resistance (see Figure 4-29, CQFP vs. PQFP).

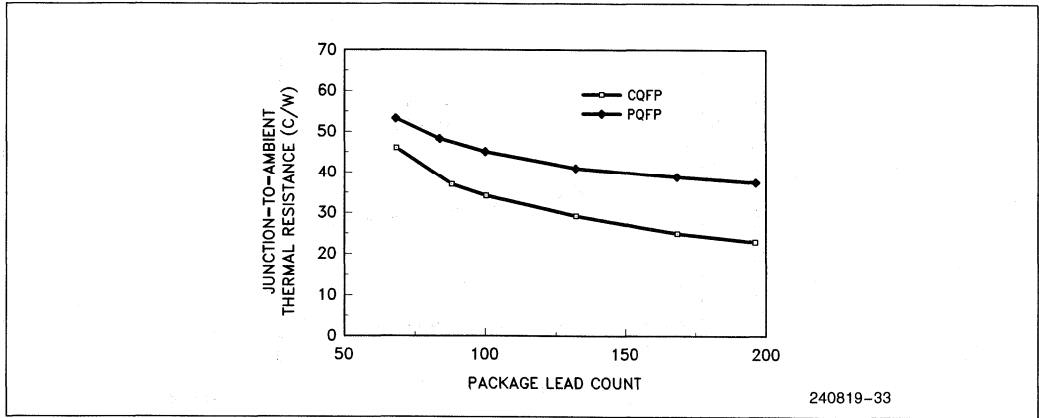


Figure 4-29. Effect of Packaging Material on Thermal Resistance

DIE SIZE

As shown in Figure 4-30, thermal resistance reduces as the die size increases. Increase in die size results in lower power density and larger effective heat transfer area. The changes in thermal resistance are sharper at smaller die sizes, and as the die size approaches package size, they become less significant.



DEVICE POWER DISSIPATION

An increase in device power, which will raise the temperature of the package, results in lower junction-to-ambient thermal resistance (θ_{ja}) values in natural convection, while not affecting θ_{ja} in forced convection. The values of θ_{jc} do not change significantly as a function of the device power both in natural and forced convection (see Figure 4-31). In natural convection, the convective heat transfer coefficient is proportional to the temperature difference between the case and the ambient. Therefore, the case-to-ambient thermal resistance will be inversely proportional to this temperature, and as a result, to the device power.

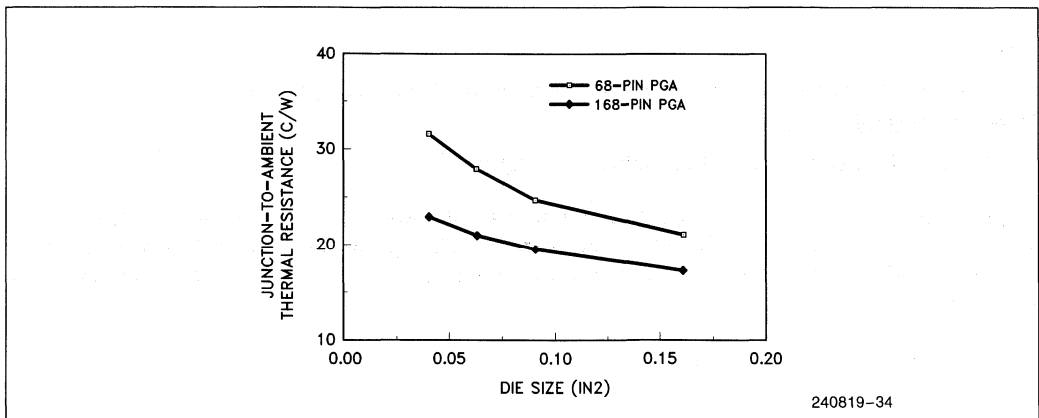


Figure 4-30. Effect of Die Size on Package Thermal Resistance

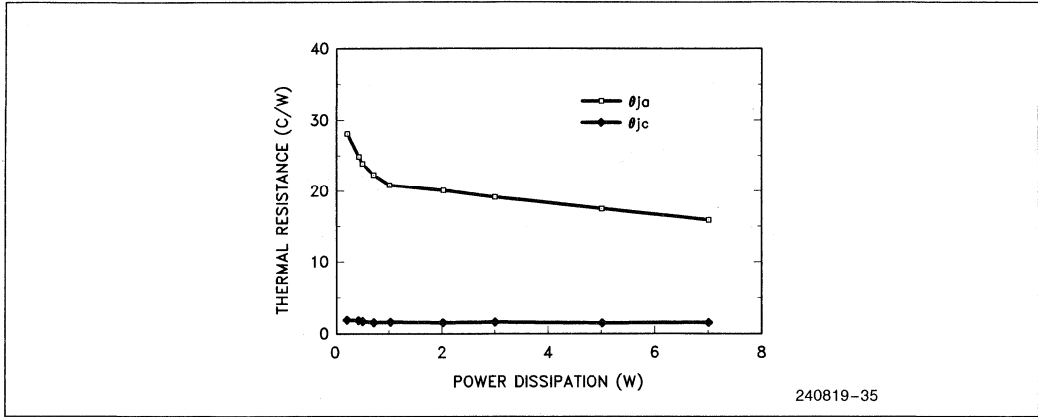


Figure 4-31. Effect of Power Dissipation on Thermal Resistance

It should be noted that the error in θ_{ja} also increases at lower power levels, because both temperature and power measurements are less accurate.

In the case of forced convection, the heat transfer coefficient does not depend on temperature explicitly. Dependency on temperature is only due to changes in material properties. These properties do not vary significantly for air within the temperature ranges normally encountered. However, at low flow rates, natural and forced convection may have effects that are of the same order of magnitude (mixed convection). In this region, a small dependency on power may be observed, but as the flow rate increases, power dependency disappears.

AIR FLOW RATE

In forced convection, case-to-ambient thermal resistance is a function of the air flow rate, as shown by Equation 11:

$$\theta_{ca} = K/V^m \tag{11}$$

$$\theta_{ja} = \theta_{jc} + K/V^m$$

where:

K = Constant depending on air properties as well as package geometry

V = Air velocity (m/s)

m = $1/2$ and $4/5$ (laminar and turbulent, respectively)

Figure 4-32 shows how θ_{ja} varies as a function of air flow rate for 168-lead PGA with and without heat fins. At lower air flow rates, there is a strong dependency of θ_{ja} on the air flow rate, but as the air flow rate increases, θ_{ja} values become less sensitive to the changes in the flow rate.

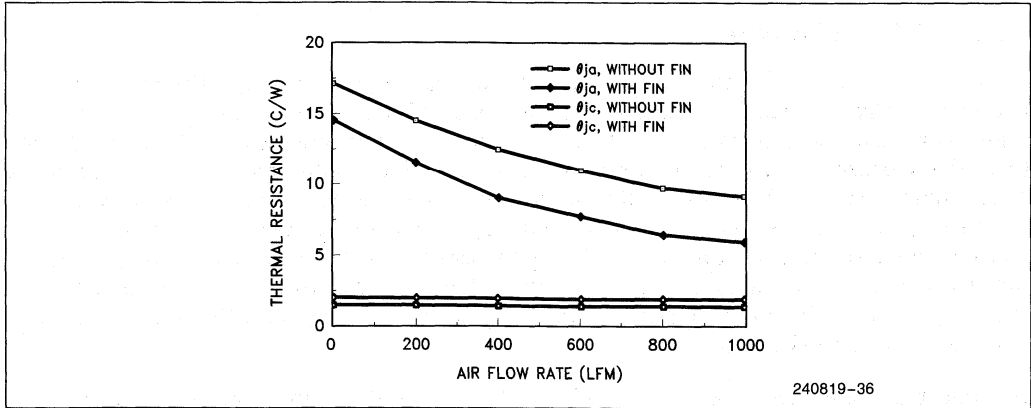


Figure 4-32. Effect of Air Flow Rate on Thermal Resistance of 168-Lead PGA Package

Mounting Parameters

PC BOARD SIZE AND THERMAL CONDUCTIVITY

Figure 4-33 shows that a printed circuit board can act as a heat fin, resulting in lower junction-to-ambient thermal resistance due to the increased heat transfer area. The effect of the board size on overall thermal resistance may vary, depending on the thermal resistance between the junction and the board compared to the resistance between the case and the ambient. Smaller packages with a relatively high case-to-ambient thermal resistance value are more dependent on the board for transfer of heat to ambient than are the larger size packages.

Another factor that impacts the thermal resistance from board to ambient is board thermal conductivity. As board thermal conductivity or board thickness increases, the spreading resistance through the board reduces, and a larger board area becomes available for heat transfer to the ambient.

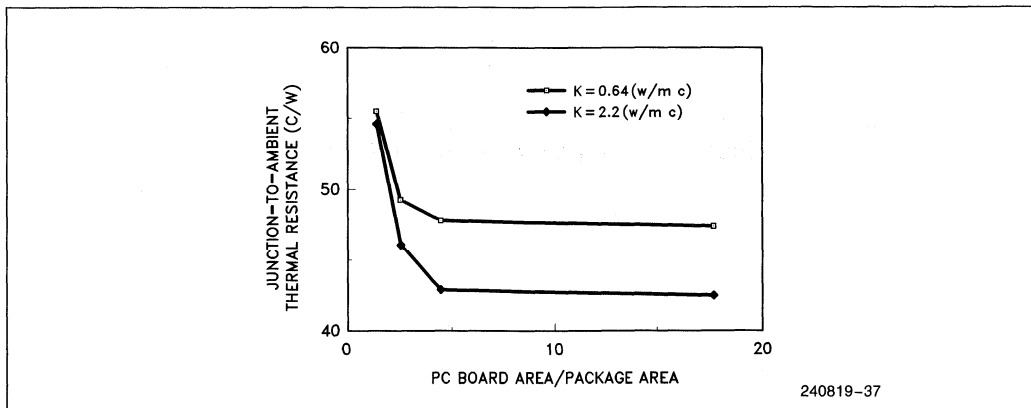


Figure 4-33. Effect of PC Board Material and Size on Thermal Resistance of 132-Lead PQFP

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PC BOARD TEMPERATURE

PC board temperature is an important parameter that impacts package thermal resistance and is normally ignored. For a board of specific size and properties with only the component under consideration mounted on it, there is a unique equilibrium temperature distribution (T_b) on the board under fixed environmental and mounting conditions. However, if there are other components on the board or the board is attached to a heat sink, the value of T_b may increase or decrease. A change in board temperature will also change junction temperature and consequently junction-to-ambient thermal resistance. This value of junction-to-ambient thermal resistance, which is different from the value measured when the board is not influenced by other heating or cooling factors (θ_{ja}), is referred to as apparent thermal resistance or systems-level thermal resistance ($\theta_{ja,s}$).

In almost all practical applications, PC boards are populated by many components, and heating of one package influences other packages. In order to get a relatively good estimate of system thermal resistance ($\theta_{ja,s}$), and as a result, of junction temperature, $\theta_{ja,s}$ and θ_{ja} values must be correlated through another parameter. As it turns out, this parameter is T_b , and by breaking up the package thermal resistance into a simple resistor network, a relation can be derived between $\theta_{ja,s}$, θ_{ja} , and T_b . Therefore, by using the correlation θ_{ja} , and by measuring T_b , junction temperature can be calculated.

Figure 4-34 shows a simple equivalent single-resistor network for any package. In this model, it is assumed that the heat path is from junction to package boundary, and from there, a portion of the heat is transferred directly to the ambient, while the rest goes to the board and is distributed and transferred to the ambient.

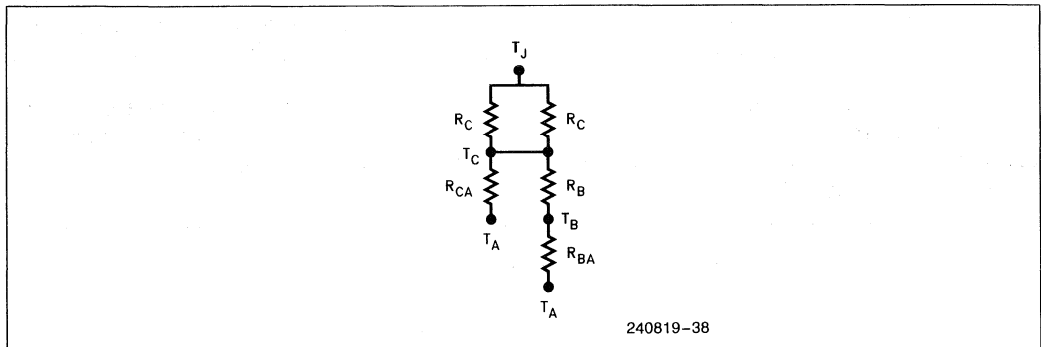


Figure 4-34. Simplified Resistor Network

It should be noted that the model shown in Figure 4-34 is simplified, and the actual package resistor network model can be more complex. The following expression shows the relation between $\theta_{ja,s}$ and θ_{ja} and board temperature rise ($T_b - T_a$):

$$\theta_{ja,s} = \theta_{ja} + S \left(\frac{T_b - T_a}{P} \right) - \frac{S R_a R_{ba}}{(R_a + R_b + R_{ba})}$$

$$S = \frac{R_a}{R_a + R_b}$$

(12)

where:

- P = Power dissipation (W)
- R_a = Case-to-ambient resistance (C/W)
- R_b = Case-to-board resistance (C/W)
- R_{ba} = Board-to-ambient resistance (C/W)
- R_c = Junction-to-case resistance (C/W)
- S = Sensitivity parameter, $R_a/(R_a + R_b)$ ($0 < s < 1$)
- $T_b - T_a$ = Board temperature rise over ambient (C)

Equation 12 shows a linear dependence of $\theta_{ja,s}$ on board temperature rise; as the board temperature increases or decreases, the system thermal resistance will increase or decrease. The rate of these changes is dictated by sensitivity parameter s, which in turn depends on R_a/R_b . As R_a/R_b increases, thermal resistance becomes more sensitive to board temperature rise; in other words, the package becomes more thermally coupled with other components on the board. Large values of R_a/R_b indicate that the package depends more on the board for transfer of heat to the ambient than on direct heat transfer to the ambient (larger packages vs. smaller packages). On the other hand, as R_a/R_b decreases, s decreases. Smaller R_a/R_b means a higher degree of insulation between the package and the board. For example, the thermal resistance of a package with a copper lead frame is more sensitive to board temperature rise than its counterpart with an Alloy 42 lead frame, as shown in Figure 4-35.

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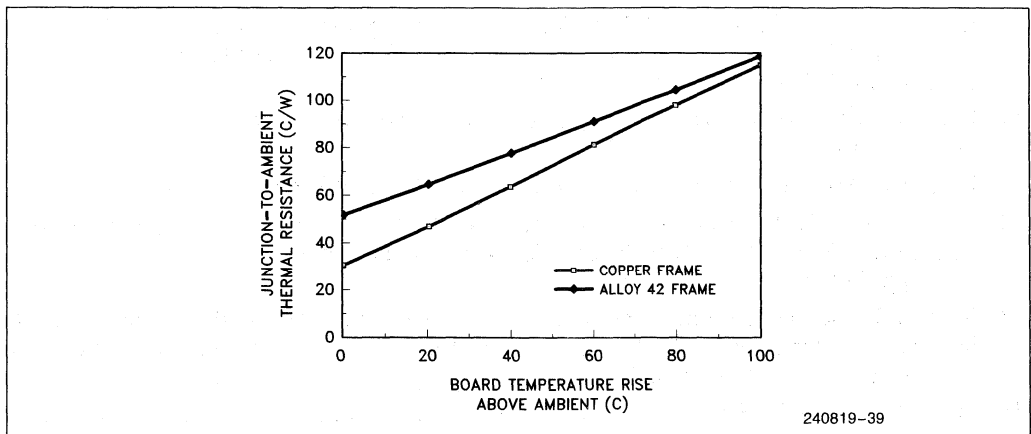


Figure 4-35. Effect of Board Temperature Rise on Thermal Resistance of 132-Lead PQFP with Copper and Alloy 42-Lead Frames

To determine sensitivity factor s and intercept B in expression 12, the package system thermal resistance can be measured under two different board temperature conditions (θ_{ja} is assumed to be known).

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Physical Constants of IC Package Material

5



CHAPTER 5 PHYSICAL CONSTANTS OF IC PACKAGE MATERIALS

The following tables list the typical physical properties of materials used in IC packages.

Table 5-1. Case Material Characteristics

Properties		Wt % Legend	Alumina	Sealing Glass	Molding Compound	Quartz Glass	Kovar
Mechanical Properties	Specific Gravity		3.6–3.9	4.7	1.79–1.85	2.16	8.36
	Modulus of Elasticity	GN/m ²	390		E ₁ = 11.7 E ₂ = 0.1	69	138
	Tensile Strength	MN/m ²	323	39	19.98	78	516.75
Thermal Properties	Thermal Conductivity	W/m°C	18	0.4–1.3	>0.5	1.4–1.7	16
	Coefficient of Thermal Expansion	10 ⁻⁶ /°C	7.0	6.3	α ₁ < 23 α ₂ < 80	0.6	4.3
Electrical Properties	Electrical Resistivity	Ωcm	>10 ¹⁴	>10 ¹¹	>10 ¹³	>10 ¹²	49 × 10 ⁻⁶
	Dielectric Constant	At 1 MHz	7.9–10	12.3	4	3.9	

Table 5-2. Lead/Lead Frame Material Characteristics

Properties		Wt % Legend	Copper Alloy MF 202	Alloy 42	Kovar
Mechanical Properties	Specific Gravity		8.88	8.12	8.36
	Modulus of Elasticity	GN/m ²	113	145	138
	Tensile Strength	MN/m ²	489 ~ 585	620 ~ 723	516 ~ 585
Thermal Properties	Thermal Conductivity	W/m°C	150	16	16
	Coefficient of Thermal Expansion	10 ⁻⁶ /°C	17	4.3	4.3
Electrical Properties	Electrical Resistivity	Ωcm	5.8 × 10 ⁻⁶	58 × 10 ⁻⁶	49 × 10 ⁻⁶

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Table 5-3. Soldering Material Characteristics

Property	Tin-Lead Plating	Tin-Lead Eutectic Solder	Tin	Gold
Melting Point (°C)	200–225	≈ 183	232	1063

WT% Legend:

GN/m²—Giga newtons per meter squared
 MN/m²—Mega newtons per meter squared
 W/m°C—Watts per meter degrees Celsius
 Ωcm—Ohms per centimeter

Surface Mount Technology/Handling and Assembly Information

6

CHAPTER 6 SURFACE MOUNT TECHNOLOGY

INTRODUCTION

Traditional through-hole methods of assembling conventional electronic assemblies have essentially reached their limits in terms of improvements in cost, weight, volume, and reliability. For increased board density, the current trend is to use surface mount technology (SMT). SMT allows production of more reliable assemblies at reduced weight, volume, and cost. As shown in Figure 6-1, the weight of printed wire assemblies (PWAs) using SMT is reduced because surface mount components (SMCs) can weigh up to 10 times less than their conventional counterparts and occupy about one-half to one-third the space on the printed wiring board (PWB) surface (see Figure 6-2). SMT also provides improved shock and vibration resistance due to the lower mass of components. The smaller lead lengths of surface mount components reduce parasitic losses and provide more effective decoupling (see Figure 6-3). The source for Figures 6-1 through 6-3 is Reference 1.

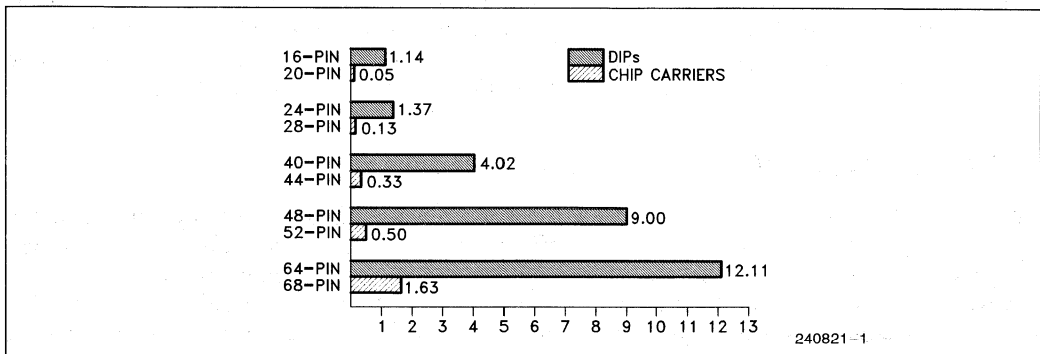


Figure 6-1. The Weight of Various Lead-Count Chip Carriers for SMT Compared to the Weight of an Equivalent DIP

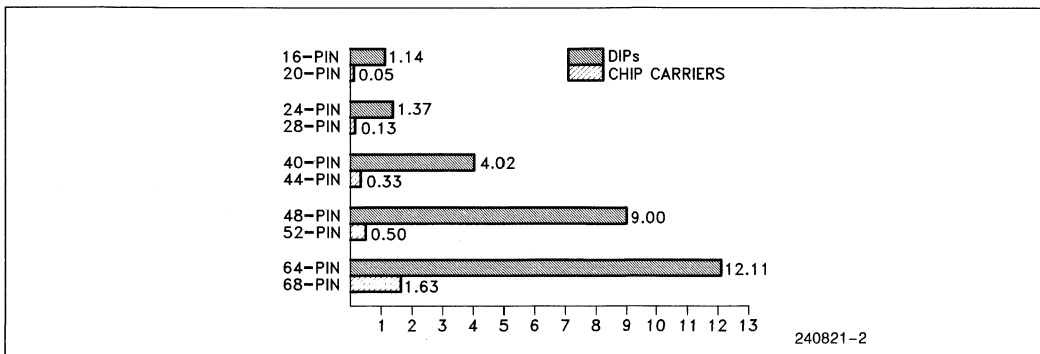


Figure 6-2. Comparison of PCB Level Area with DIP Packaging and SMT Packaging (Leadless Ceramic Chip Carriers and Small Outline Packages). SMT Results in a Significant Reduction on Board Area.

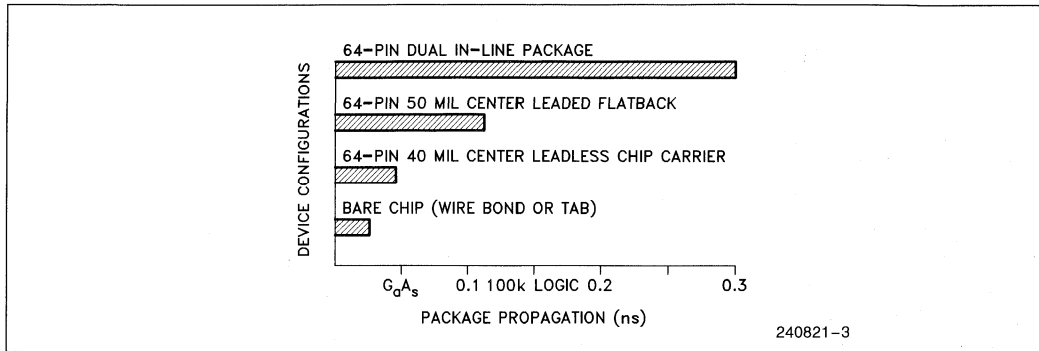
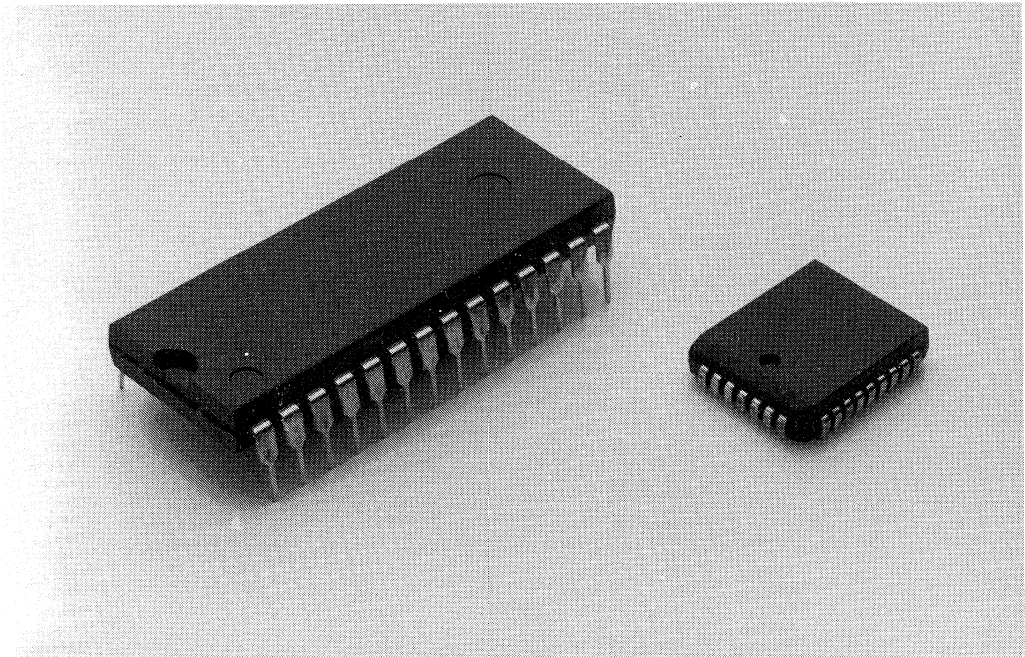


Figure 6-3. Comparison of the Propagation Delays of a Leadless Ceramic Chip Carrier and a DIP

The smaller size of SMCs and the option of mounting them on either or both sides of the PWB can reduce board real estate by four times. For example, half a megabyte of 256K DRAM memory with conventional DIP components will require about 4.0 x 4.0 in. of PC board area. The same board with surface mount components attached on a single side can accommodate one megabyte of memory. A cost savings of 30% or better can also be realized through a reduction in material and labor costs associated with automated assembly.

TYPES OF SURFACE MOUNT TECHNOLOGY

SMT is a relatively new packaging technology that replaces through-hole by surface mount components. The assembly is soldered by reflow (vapor phase/infrared) and/or wave soldering processes depending on the mix of surface mount and through-hole mount components. Figure 6-4 shows an example of a surface mount active plastic leaded chip carrier (PLCC) and its conventional leaded equivalent. When attached to PWBs, both active and passive SMCs form three major types of SMT assemblies, commonly referred to as Type I, Type II, and Type III (see Figure 6-5).



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Figure 6-4. Surface Mount Active Components and its Conventional Equivalent

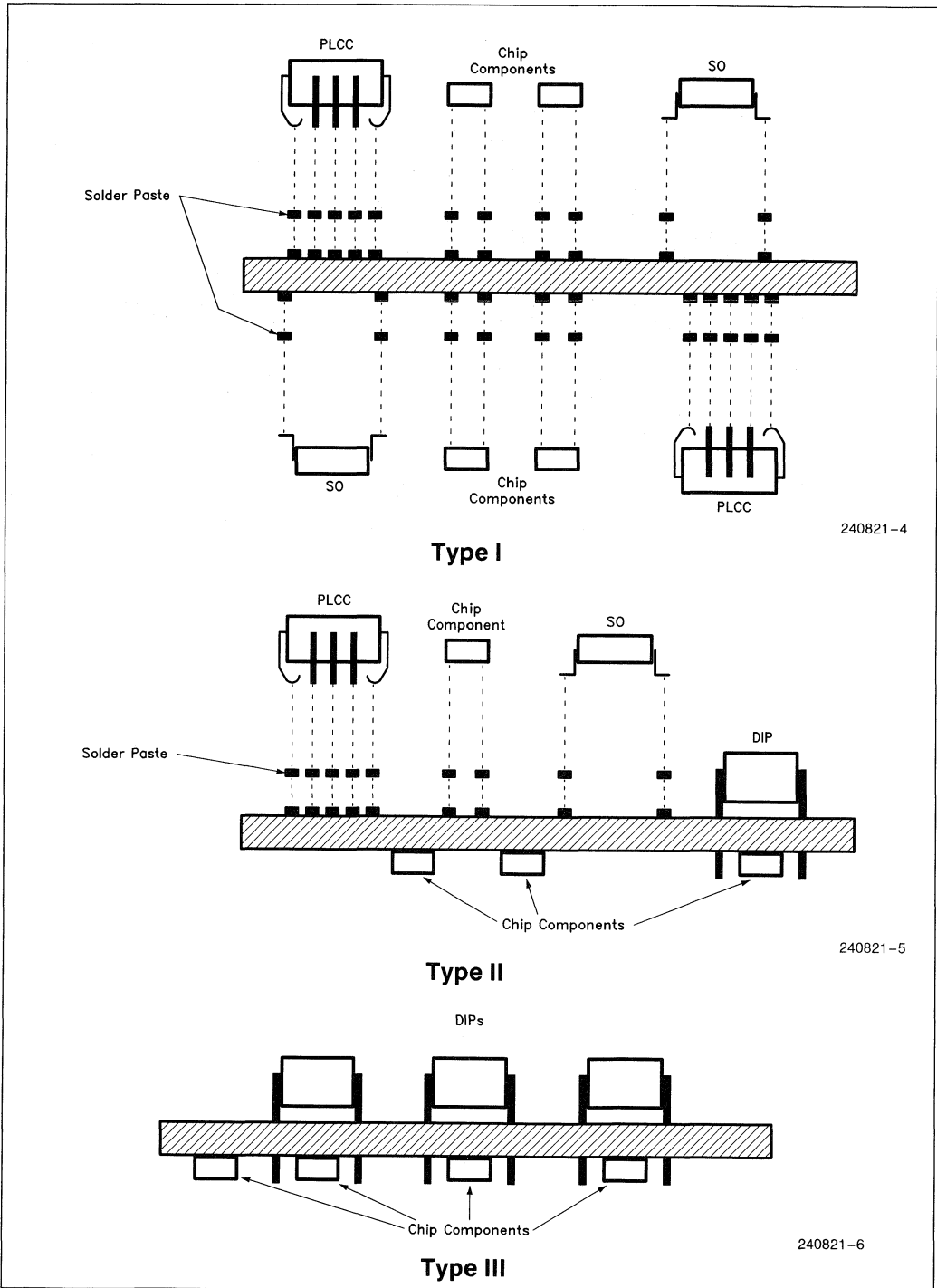


Figure 6-5. Surface Mount Technology Board Types

The process sequence for Type III SMT is shown in Figure 6-6. Leaded components are auto-inserted using existing equipment. The assembly is turned over, and adhesive is applied. Next, passive SMCs are placed by a “pick-and-place” robot, the adhesive is cured, the assembly is turned over, and the wave-soldering process is used to solder both leaded and passive SMCs in a single operation. Finally, the assembly is cleaned, inspected, repaired if necessary, and tested. Note that only passive chip components are surface mounted by exposure to solder wave.

The process sequence for Type I SMT is shown in Figure 6-7. Solder paste is screened, components are placed, and the assembly is baked to drive off volatiles from the solder paste. Currently, pastes are available that do not require baking. Finally, the assembly is reflow soldered (vapor phase or infrared) and solvent cleaned. For double-sided Type I SMT assemblies, the board is turned over, and the process sequence just described is repeated.

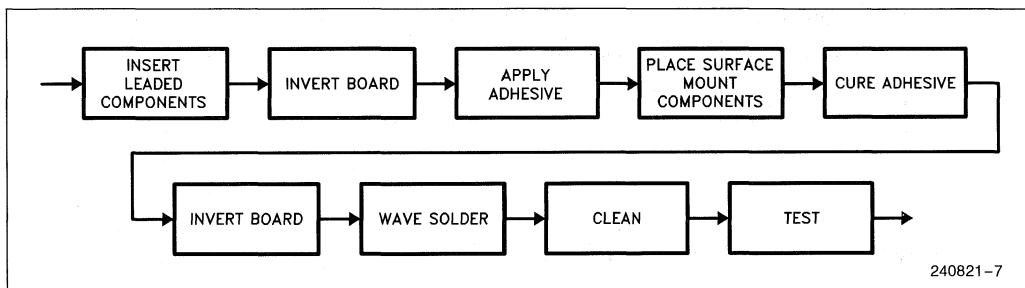


Figure 6-6. Typical Process Flow for Underwire Attachment (Type III SMT)

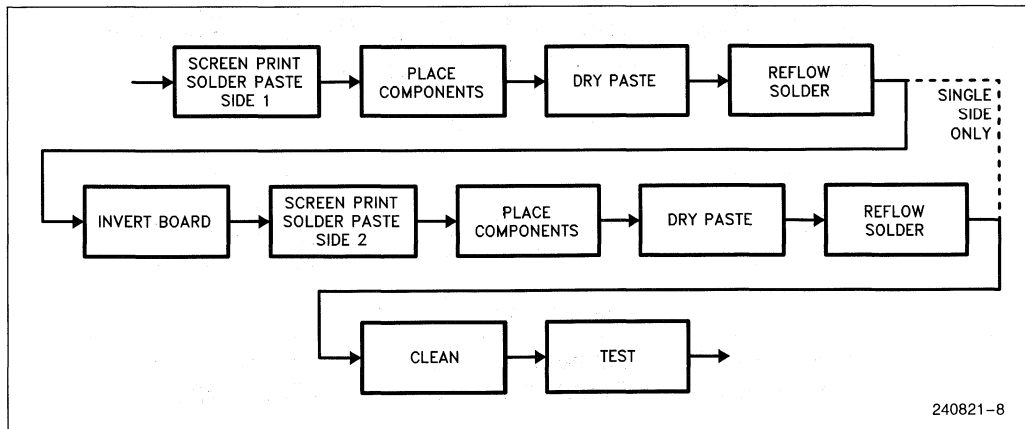


Figure 6-7. Typical Process Flow for Total Surface Mount (Type I SMT)

Type II assemblies go through the process sequence of Type I SMT followed by the sequence for Type III, as Figure 6-8 illustrates. Note that only passive chip components are exposed to solder wave immersion.

There are three major process steps in the manufacturing of electronic assemblies: component mounting, soldering, and cleaning. For conventional as well as surface mount assemblies, the equipment required for each process step is shown in Figure 6-9. The equipment shown in “single box” in this figure is for conventional assemblies, and in “double box” for SMT. If Type III equipment is properly selected, it can be used for Type I and Type II SMT when the decision is made to move into those technologies.

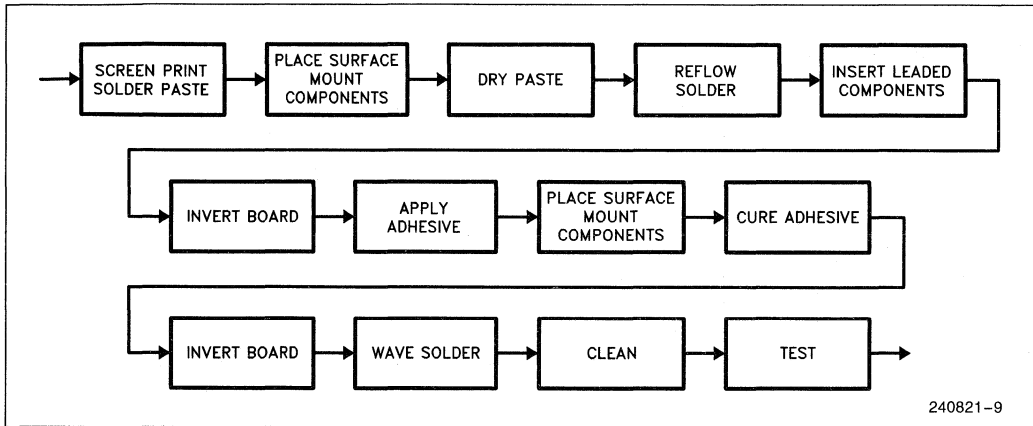


Figure 6-8. Typical Process Flow for Mixed Technology (Type II SMT)

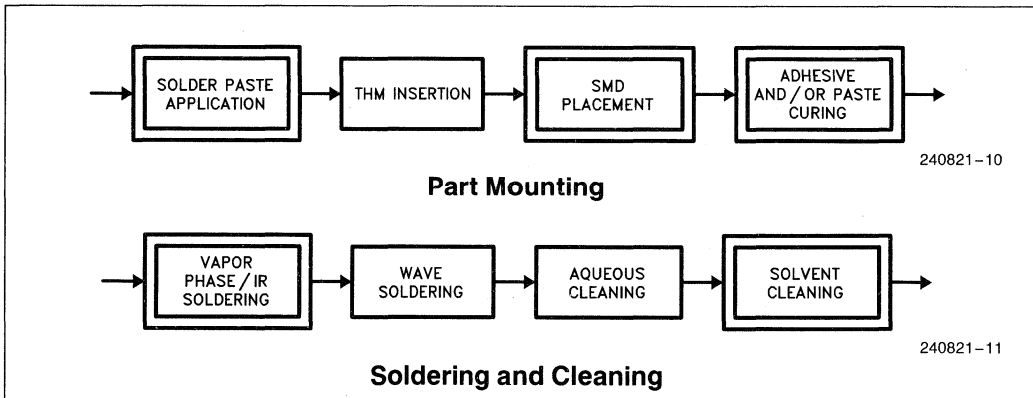


Figure 6-9. Major Equipment for Conventional (Single Box) and Surface Mount (Double Box) Assemblies (Type II SMT)

SMT manufacturing is modular in nature, and the full SMT capability can evolve in steps as needed. A line set up for Type II can be used for both Type I and Type III SMT.

SURFACE MOUNT DESIGN

Land Pattern Design

The surface mount land patterns, also called footprints or pads, define the sites where components are to be soldered to the PC board. The design of land patterns is very critical, because it determines solder joint strength and thus the reliability of solder joints, and also impacts solder defects, cleanability, testability, and repair/rework. In other words, the very producibility or success of SMT is dependent upon the land pattern design.

The lack of standardization of surface mount packages has compounded the problem of standardizing the land pattern. There are a variety of package types offered by the industry, and the variations in a given package type can be numerous. For example, for the small outline package (SOP), there are not only two lead types (gull-wing and J-lead), but there are two body types (narrow and wide). In addition, the tolerance on components varies significantly, adding to the manufacturing problems for SMT users.

In this section, we will present general guidelines for land pattern design that accommodate reasonable tolerances in component packages, process, and equipment used in manufacturing. These guidelines are based on manufacturability and environmental testing of different land pattern designs for reliability.

A desirable requirement is that the land pattern design be transparent to the soldering process used in manufacturing. This reduces the number of pad sizes in the computer-aided design (CAD) library—some CAD systems limit the total number of different pad sizes, but this may change with newer releases of CAD software—and is less confusing for the CAD designer.

Also, the designer can use the land pattern document to establish standard configurations for both manual and CAD systems.

To simplify the land pattern design guidelines, we have divided surface mount components into three different categories: (1) passive components; (2) J-lead plastic leaded chip carriers (PLCCs), including small outline J-leads (SOJs) and leadless ceramic chip carriers (LCCCs); and (3) gull-wing lead small outline packages (SOPs), including surface mount R-packs. Instead of providing specific pad sizes, the general formulas for the land pattern design applicable to the second and third categories are shown in Figures 6-10, 6-11 and 6-12. The formulas were developed based on reliability and producibility data. Each has a constant, K , which can be used to determine the exact land pattern for any size package in that category. References 2, 3, and 4 provide the details on land pattern design.

Table 6-1. Typical Board Footprint Area for PLCC

	Lead Count	A (Width) (Inch)	B (Length) (Inch)
Square	20	0.420	0.420
	28	0.520	0.520
	44	0.720	0.720
	52	0.820	0.820
	68	1.020	1.020
Rectangular	84	1.220	1.220
	28	0.420	0.620
	32	0.520	0.620

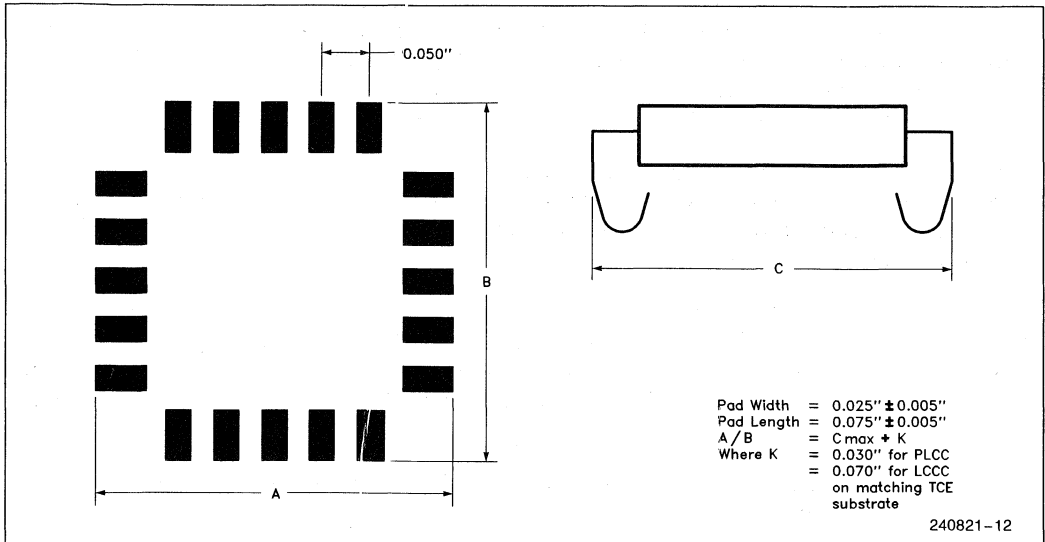


Figure 6-10. Typical PLCC, LCCC Footprint for Board Layout, Square and Rectangular Package

Table 6-2. Typical Board Footprint Area for PQFP

Lead Count	A (Width) (Inch)	B (Length) (Inch)
84	0.800	0.800
100	0.900	0.900
132	1.100	1.100
164	1.300	1.300
196	1.500	1.500

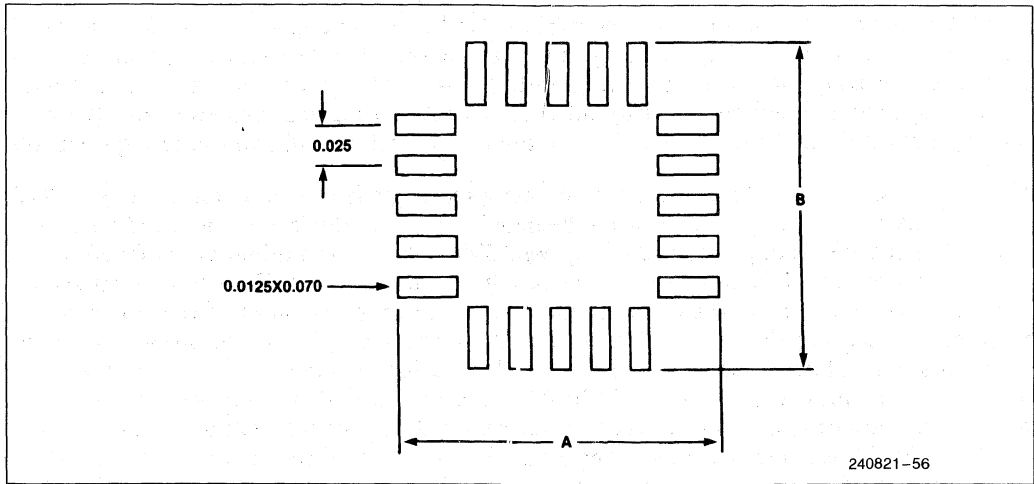


Figure 6-11. Typical PQFP Footprint for Board Layout

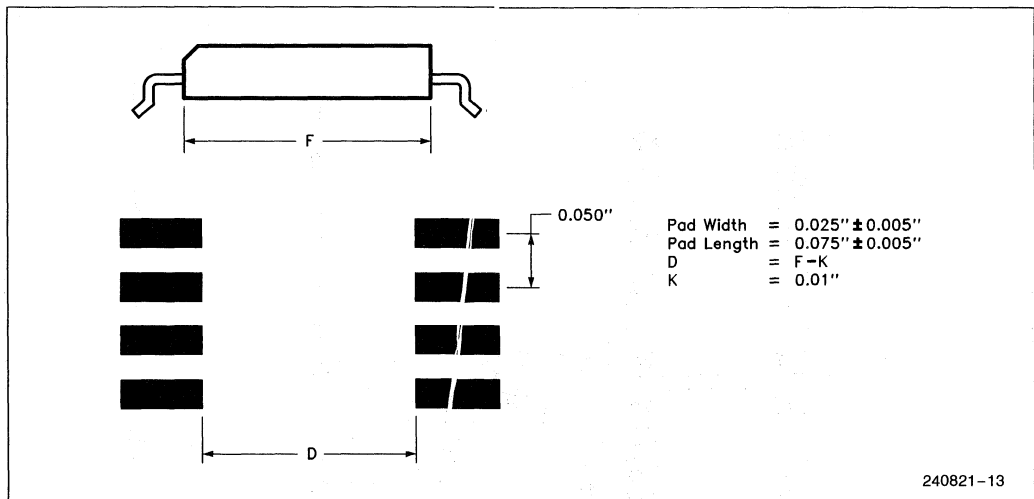


Figure 6-12. Formulas for R-Packs and SOIC Land Pattern Design

Design for Manufacturability

Design for manufacturability is gaining more recognition as it becomes clear that cost reduction of printed wiring assemblies cannot be controlled by manufacturing engineers alone. Design for manufacturability—which includes considerations of land pattern, placement, soldering, cleaning, repair, and test—is essentially a yield issue. Thus, companies planning surface mount products face a serious problem in creating manufacturable designs, generally working by trial and error and at a considerable expense. Achieving decent yield can be a source of constant irritation and often total frustration.

Of all the issues in design for manufacturability, land pattern design—discussed in the previous section—and interpackage spacing are most important. Interpackage spacing controls cost-effectiveness of placement, soldering, testing, inspection, and repair. A minimum interpackage spacing is required to satisfy all these manufacturing requirements, and the more spacing provided, the better. The following guidelines meet manufacturability requirements.

Figure 6-13 shows the interpackage spacing between the pads (not component body or lead) of SMCs, as well as the spacing between the pads of adjacent SMCs and conventional components. The spacing from pad to pad of adjacent SMCs should be a minimum of 0.050 in. For PLCCs, this means 0.075 in. between leads of adjacent components. For components such as SOJs and passives, where leads or terminations are on only two sides of the packages, the interpackage spacing should be 0.050 in. for SOJs, and 0.040 in. for passives between the adjacent sides without leads or terminations. The spacing between the pads of conventional and surface mount components should be 0.060 in. to allow enough—at least a 0.100-in.—gap for auto-insertion equipment used for conventional components. Clear spaces of at least 0.050 in. should be allowed around all edges of the PC boards if the boards are tested off the connector, or of 0.100 in. if vacuum seal is used for testing, such as bed-of-nails. These specified requirements are absolute minimum.

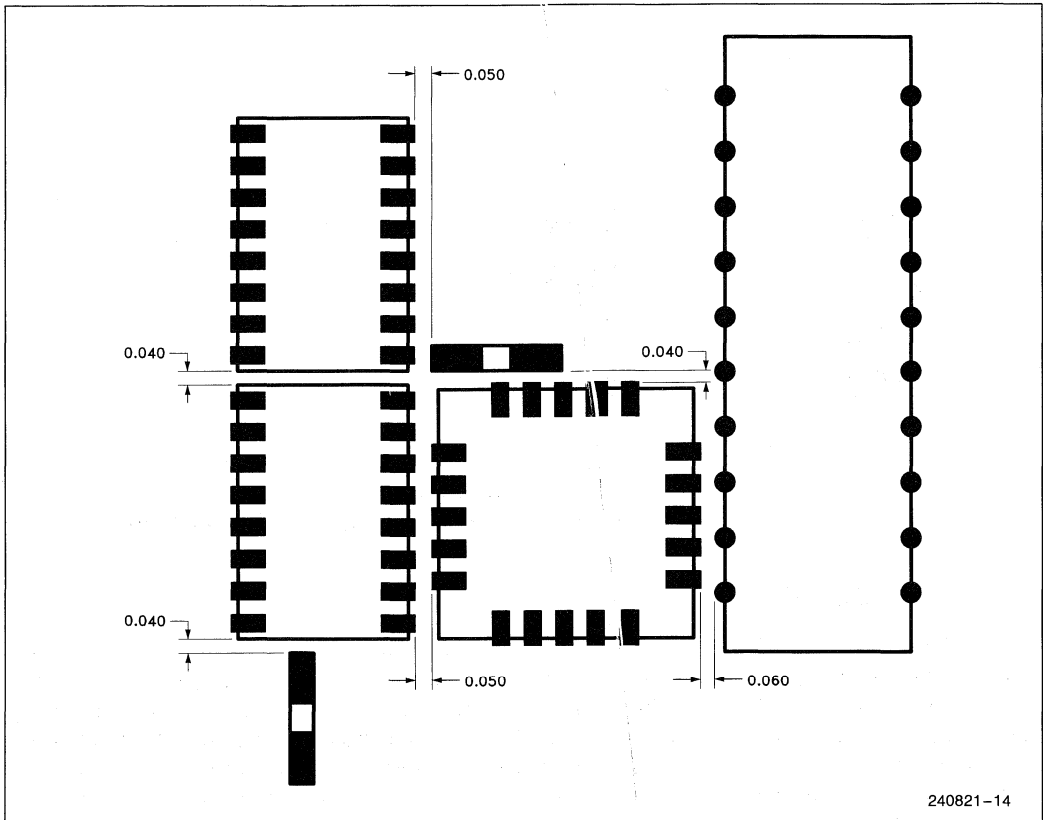


Figure 6-13. Minimum Land-to-Land Clearance between Component (Surface Mount and DIP) Lands

The interpackage spacing guideline just discussed may cause problems in some cases if the repair tool used in manufacturing does not use a vacuum tip for component removal and replacement during repair/rework. This problem may disappear when repair/rework with vacuum pick-up (removal and replacement) capability becomes available for both passive and active components. Currently, most of the hot-air repair/rework tools are intended only for active devices.

Another manufacturing consideration is the alignment of components on the PC board. Similar types of components should be aligned in the same orientation for ease of component placement, inspection, and soldering.

Via holes are used to connect SMC lands to conductor layers. They may also be used as test targets for bed-of-nails probes and/or rework ports. Via holes may be covered with solder mask material if they are not required for node testing or rework. Such vias are called tented vias.

Via holes may be placed under surface mount components. However, in Type II and Type III SMT (mix-and-match surface mount), via holes under SMCs should be minimized or tented with solder mask to prevent trapping of flux under the packages during wave soldering. For effective cleaning, via holes should be located beneath SMCs in Type I SMT assemblies (full surface mount) that will not be wave soldered.

Via holes within reflow-soldered pads should be avoided because solder can flow inside these vias during reflow soldering, causing insufficient solder fillets. Designing wide traces connected to solder pads produces the same effect as flush vias on solder pads—insufficient solder fillets.

Chapters 5, 6, and 7 in Reference 4 provide details on design for manufacturability.

Design for Testability

In SMT boards, designing for testability requires that test nodes be accessible to automated test equipment (ATE). This requirement naturally has an impact on board real estate. In addition, it impacts cost, which is dependent upon defects. A lower number of test nodes can be tolerated when defect rates are low, but higher defect occurrence demands adequate diagnostic capability by allowing ATE access to all test nodes.

Most companies use bed-of-nails in-circuit testing for conventional assemblies. Use of SMCs does not impact testability if the rule for testability of assemblies is strictly observed. This rule requires that (1) 0.050-in. and 0.100-in. test probes are used, (2) solder joints are not probed, and (3) through-hole vias or test pads are used to allow electrical access to each test node during in-circuit testing. If possible, this electrical access should be provided both at top and bottom, and bottom access is necessary. The main drawback of providing all the required test pads is that the real estate savings offered by SMT are somewhat compromised. To retain the real estate savings offered by SMT requires development of some form of self-test or reliance upon functional tests only. However, self-test requires considerable development effort and implementation time, and functional tests lack the diagnostic capability of in-circuit tests.

Designing for manufacturability, test, and repair are very important for yield improvement and thus cost reduction. Design for manufacturability and test essentially impacts SMT real estate savings. If processes are brought under control, the need for repair and test will become less of an issue, but until then, some real estate benefits provided by SMT and easily producible surface mount boards will be sacrificed. The following sections address process issues in the manufacturing of surface mount assemblies that play a critical role even when boards are designed for manufacturability.

SUBSTRATE PREPARATION: ADHESIVE, SOLDER PASTE APPLICATION

Solder Application, Paste, and Preform

Solder paste plays an important part in reflow soldering (Type I and Type II SMT). The paste acts as an adhesive before reflow and even may help align skewed parts during soldering. It contains flux, solvent, suspending agent, and solder of the desired composition. Characteristics such as viscosity, dispensing, screening, flow, and spread are key considerations in selecting a particular paste. Susceptibility of the paste to solder ball formation and wetting characteristics are also important selection criteria.

Solder paste is applied on the solder pads before component placement by screening, stenciling, or syringe. Screens are made from stainless steel or polyester wire mesh, and stencils are etched stainless steel or brass sheets. Stencils are preferred for high-volume product runs, because they are more durable than screens, are easier to align, and can apply a thicker layer of solder paste. Because they are more expensive than screens, they may not be suitable for small production runs.

Solder preforms, also called doughnuts, are sometimes used for through-hole mounted devices. They are available in required size and composition with flux inside or as a coating, or without flux. They may be cost-effective if there are only a few leaded components on the board. Only the reflow (vapor phase/infrared) process can be used for both through-hole leaded and surface mount components.

SURFACE MOUNT COMPONENTS AND THEIR PLACEMENT

Component Packaging

All active components are not currently available in surface mount, which will keep us in mix-and-match format for some time to come. However, the situation is changing very rapidly.

Intel active components are available in tubes or magazines, as well as on tapes and reels. Tapes and reels will be the most popular packaging methods because they preserve lead coplanarity. The EIA specification RS-481A has standardized 7-in. reels for passive components and 13-in. reels for active components.

Component Placement

Requirements for accuracy make it almost mandatory to use auto-placement machines for placing surface mount components on the PC board. Selection of the appropriate auto-placement machine is dictated by the type of parts to be placed and their volume. As shown in Figure 6-14, there are basically four types of auto-placement machines available on the market today: (1) in-line, (2) simultaneous, (3) sequential, and (4) sequential/simultaneous placement equipment.

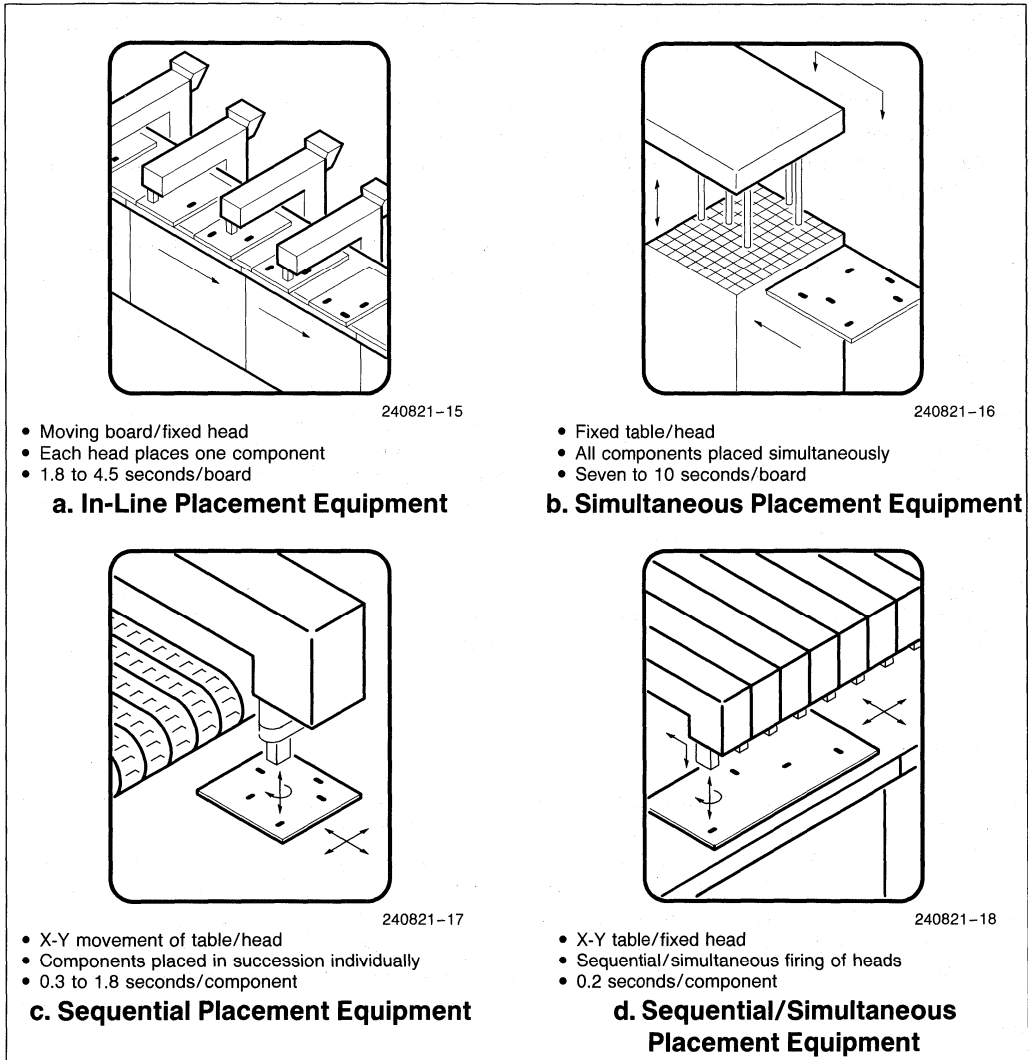


Figure 6-14. Four Major Categories of Placement Equipment—(a) In-Line Placement, (b) Simultaneous Placement, (c) Sequential Placement, and (d) Sequential/Simultaneous Placement Equipment

Shown in Figure 6-14a, in-line placement equipment employs a series of fixed-position placement stations. Each station places its respective component as the PC board moves down the line. Cycle times vary from 1.8 to 4.5 seconds per board.

Illustrated in Figure 6-14b, simultaneous placement equipment places an entire array of components onto the PC board at the same time. Typical cycle times vary from seven to 10 seconds per board.

Sequential placement equipment, shown in Figure 6-14c, typically utilizes a software-controlled X-Y moving table system. Components are individually placed on the PC board in succession. Typical cycle times vary from 0.3 to 1.8 seconds per component.

Sequential/simultaneous placement equipment, illustrated in Figure 6-14d, features a software-controlled X-Y moving table system. Components are individually placed on the PC board from multiple heads in succession. Simultaneous firing of heads is possible. Typical cycle times vary, with an average of 0.2 seconds per component.

Many models of auto-placement equipment are available in each of the four categories. Selection criteria should consider such issues as what kind of parts are to be handled; whether they come in tube, magazine, or on a tape; and whether the machine can accommodate future changes in tape sizes. Selection and evaluation of tapes from various vendors for compatibility with the selected machine is very important. Off-line programming, teach mode, and edit capability, as well as ECAD/CAM compatibility may be very desirable, especially if a company has already developed an ECAD/CAM database. Special features such as vision capability, adhesive application, component testing, board handling, and capability for further expansion may be of interest for many applications. Vision capability is especially helpful in accurate placement of fine-pitch packages. Reliability, accuracy of placement, and easy maintenance are important to all users.

Reference 4 provides the details on selection criteria for pick-and-place equipment. Since pick-and-place equipment constitutes the major portion of the capital investment required for SMT manufacturing lines, a detailed evaluation is essential before purchasing a particular machine.

SOLDERING

Like the selection of auto-placement machines, the type of soldering process required depends upon the type of components to be soldered and whether leaded and leadless parts will be combined. For example, if all components are surface mount types, the reflow method (vapor phase or infrared) may be desirable. However, for a combination of leaded and surface mount components, reflow soldering for surface mount components followed by wave soldering for through-hole mount components is optimum. No process is best for all soldering tasks. For example, in infrared reflow, both the heating and cooling rates of assemblies can be controlled more precisely than in vapor phase. This has a direct impact on solder defects, as discussed later.

Vapor Phase Soldering

Vapor phase soldering, also known as condensation soldering, uses the latent heat of vaporization of an inert liquid. The latent heat is released as the vapor condenses on the part to be soldered. The soldering temperature is constant and is controlled by the type of fluid. Thus, unlike wave, infrared, and laser soldering, vapor phase soldering does not require control of the heat input to the solder joints or to the PC board. It heats independent of the part geometry, heats uniformly, and does not exceed the fluid boiling temperature. The process is also suitable for soldering odd-shaped parts, flexible circuits, and pins and connectors, as well as for reflow of tin-lead electroplate and surface mount packages. However, all these features make vapor phase soldering an easily automated process. It does not require the fluxing, preheating, and soldering adjustments so critical in other processes. Since heating is by condensation, the rate of temperature rise depends on the mass of the part. Therefore, leads on packages heat up faster than the component body or solder pads. With leaded components, this can lead to the wicking of solder paste up the lead, causing open solder joints. Vapor phase soldering also has other process-related problems, such as solder balls, part movement, and damage to temperature-sensitive parts. Maximum temperature ramps rate can be controlled through the use of a preheat zone. For moisture sensitive PSMC a maximum allowable ramp rate has been recommended—see Table 6-4.

Both in-line and batch-type systems are available. The in-line system is suitable for mass production. For low-volume production or for research and development, a batch process is generally used. A schematic of a batch-type process is shown in Figure 6-15, and an in-line process in Figure 6-16. For both processes, the major disadvantages are price of the liquid, vapor loss, and parts movement (which can be advantageous for part alignment). The batch process minimizes vapor loss by using a less expensive secondary fluid as a blanket over the primary fluid. The cooling coils shown in Figure 6-16 are also intended to minimize vapor loss.

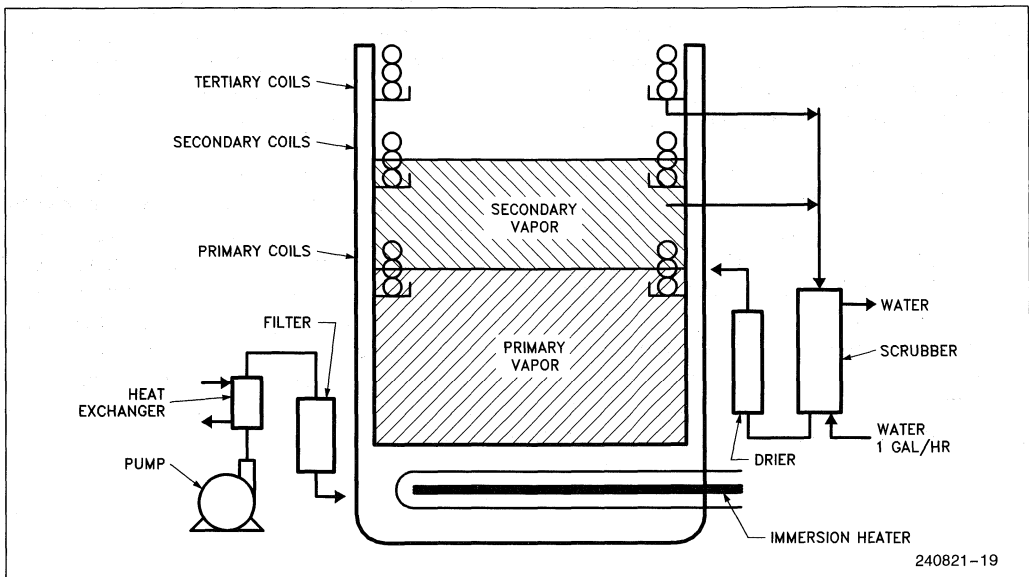


Figure 6-15. Schematic—Batch-Type Vapor Phase Soldering System for SMT

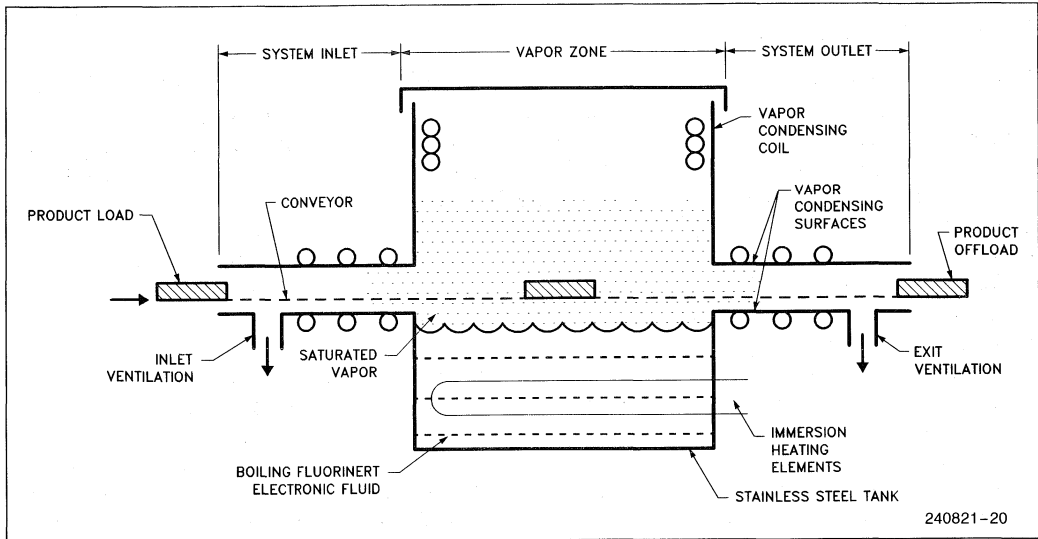


Figure 6-16. Schematic—In-Line Vapor Phase Soldering System for SMT

Infrared Reflow Soldering

In infrared (IR) reflow soldering, radiant or convective energy is used to heat the assembly. There are basically two types of IR reflow processes: focused (radiant) and non-focused (convective). The latter is proving to be more desirable for SMT. Focused IR radiates heat directly on the parts and may heat assemblies unevenly. The heat input on the part may also be color-dependent. In non-focused or diffused IR, the heating medium can be air, an inert gas, or simply convection energy. A gradual heating of the assembly is necessary to drive off volatiles from the solder paste. The gradual heating of boards is accomplished by various top and bottom heating panels, as shown in Figure 6-17. After an appropriate time in preheat, the assembly is raised to the reflow temperature for soldering and then cooled. The solder paste used for vapor phase may not necessarily be suitable for the IR process.

The IR reflow process is generally considered more suitable for gull-wing than J-lead packages. With the advent of diffused IR, J-lead packages are also being successfully soldered by many companies. There is concern that packages supplied by some companies may not be compatible with certain IR ovens. The advantage of IR over vapor phase is that, if properly designed, it can be used for baking adhesive and paste, and for reflow soldering. Another key advantage of IR over vapor phase is the operating cost. Also, the incidence of solder joint openings due to lead coplanarity is less frequent in the IR process than in vapor phase (see References 4 and 5). As in the case of VPS a maximum temperature ramp rate has been recommended for moisture sensitive PSMC—see Table 6-4. Because of these reasons, the IR process is becoming very popular in the United States.

Laser Reflow Soldering

Laser soldering is a relative newcomer to soldering technology. It complements other soldering processes rather than replacing them, and like vapor phase and IR soldering, lends itself well to automation. It is faster than hand soldering but not as fast as wave, vapor, or IR soldering. Heat-sensitive components that might be damaged by vapor phase or IR can be soldered easily by laser since only the leads are heated to reflow temperature. In laser soldering, the process problems involve potential damage to adjacent components if laser beam width is not properly adjusted.

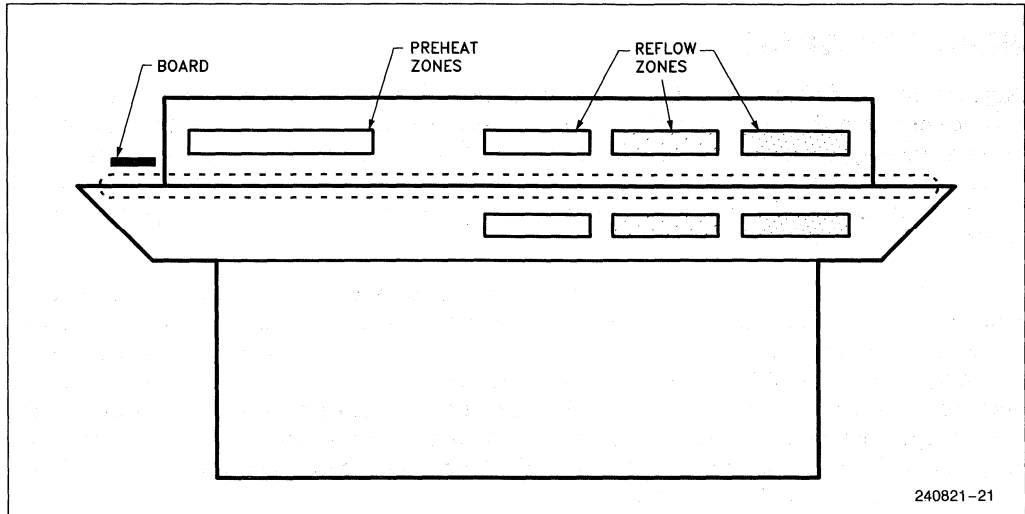


Figure 6-17. Schematic—In-Line Infrared (IR) Soldering System for SMT

CLEANING

In general, cleaning of SMT assemblies is harder than that of conventional assemblies because of smaller gaps between surface mount components and the PWB surface. The smaller gap can entrap flux, which can potentially cause reliability problems if the PWB is not properly cleaned. Thus, the cleaning process depends upon the spacing between component leads, spacing between component and substrate, the source of flux residue, and the soldering process. Most companies use synthetic or rosin-based fluxes generally known as rosin activated (RA), rosin mildly activated (RMA), synthetic activated (SA), or synthetic mildly activated (SMA). Stabilized halogenated hydrocarbon/alcohol azeotropes, such as freon TMS, are the preferred solvents for removal of synthetic and rosin-based flux residues.

Some companies successfully use organic acid (OA) flux for wave soldering of passive surface mount components glued to the bottom of the board (see Reference 6). Residues from OA fluxes are generally removed with water. Success of this technique is usually directly proportional to the amount of adhesive filling the potential entrapment area under the component and pressure of the water jets in the cleaner. Use of water-soluble fluxes may increase in the future because they are environmentally more desirable. Also, due to recent efforts to reduce

chlorofluorocarbons (CFCs) to prevent ozone layer depletion, water-soluble fluxes and solvents with lower CFCs will become almost mandatory. Environmental concern is also driving the usage of water-soluble solder paste, which may become very common in the future.

One of the key issues in SMT has been to determine cleanliness of SMT assemblies, because the conventional Omega meter test used for DIP boards may not be adequate. For this reason, the industry is trying to standardize on surface insulation resistance (SIR) surface mount boards. The current industry standard for board cleanliness is 100-megohm SIR after cleaning, regardless of which flux or cleaning method is used.

REPAIR/REWORK

Repair/rework of SMT assemblies is easier than that of conventional components. Due to the absence of plated through-holes, these components are easier to remove, and the possibility of thermal damage is nonexistent. A number of tools are available for removing components, including hot-air devices for removing active surface mounted components. A key issue in using hot-air devices is preventing thermal damage to the component or adjacent components.

No matter which tool is used, all the controlling desoldering/soldering variables need to be addressed, including the number of times a component can be removed and replaced, desoldering temperature and time, and damage to PWAs. It is also very helpful to preheat the assembly at 150°F–200°F for 15 to 20 minutes before rework to prevent thermal damage such as measling or white spots of the boards, and to avoid pressure on pads during the rework operation (see Reference 7). To prevent moisture induced damage, SMT components may require bake-out prior to removal from the board. The guidelines outlined in the Dessicant Pack Section should be followed.

TECHNICAL ISSUES IN FINE PITCH

The need for high lead-count packages in semiconductor technology has increased with the advent of application-specific integrated circuit (ASIC) devices. As the package lead count increases, devices will get larger and larger. To ensure that the area occupied by packages remains within limits of manufacturing equipment, lead pitches will have to be reduced. This—coupled with the drive toward higher functional density at the board level for enhanced performance and miniaturization—has fostered the introduction of many devices, such as Intel's 386™ SX microprocessor, in fine-pitch surface mount packages.

A fine-pitch package can be broadly defined as any package with a lead pitch finer than the 50-mil lead pitch of standard surface mount packages as PLCCs and SOPs. Most common lead pitches are 25 mils, but lower pitch devices are also becoming available.

There are two different versions of fine-pitch packages: those with corner bumpers and those without. Versions without bumpers are called quad flatpacks (QFPs); those with bumpers are referred to as plastic quad flatpacks (PQFPs). The QFP types have a very low stand-off height, making it very difficult to clean assemblies containing these packages.

The assembly process most dramatically affected by the fine-pitch package is component placement. Placement of any surface mount package with 25 mils or less of lead pitch must be made with the assistance of a vision system for accurate alignment.

Placement vision systems typically consist of two cameras. The top camera system scans the surface of the board and locates three fiducial targets that are designed into the artwork of the board. The placement system then offsets the coordinates in the computer for any variation in true board location. The bottom camera system, located under the placement head, views the component leads. Since the leads of fine-pitch components are too fragile to support mechanical centering of the device, the vision system automatically offsets for variations in the X, Y, and theta dimensions. This system also inspects for lead integrity problems, such as bent or missing leads.

The manufacturing issues for assembling fine-pitch components on PC boards also include (1) printing various amounts of solder paste on the 25-mil and 50-mil lands, (2) soldering and inspecting the fine-pitch leads and solder joints, (3) reworking defective devices, (4) cleaning adequately under and around package leads, (5) baking of the packages to remove moisture, and (6) handling of the packages without damaging fragile leads. These challenges are by no means insurmountable, but require investment in capital and engineering resources.

CONCLUSION

The major technical considerations for implementing SMT include surface mount land pattern design, design for manufacturability, components and their placement, adhesive-application wave soldering, reflow soldering, cleaning, and repair/rework. These considerations must be taken into account and thoroughly understood before converting to SMT. Surface mount technology is revolutionary, and for most companies, requires a complete rethinking of design and manufacturing processes, including the software and tool methodologies used to support them. SMT is not a technology of tomorrow, but a technology of today. Intel has made the investment in SMT for component, board, and system products to keep customers on the leading edge.

DESICCANT PACKING (BAKE AND BAG) METHODS AND MATERIALS

6

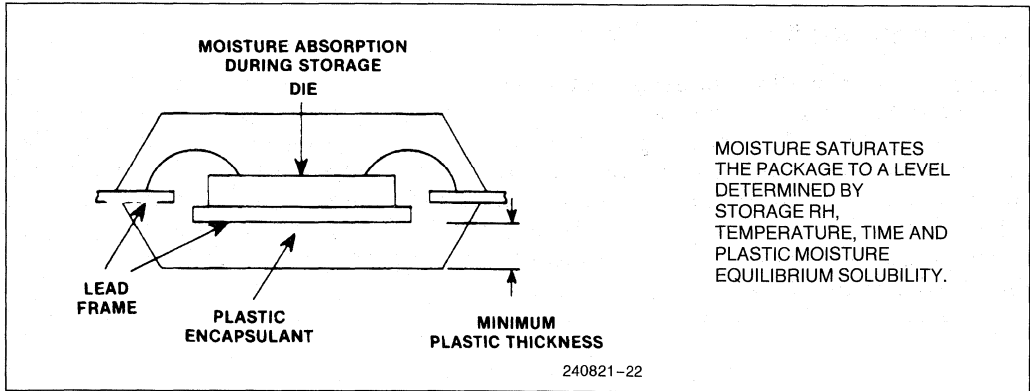
INTRODUCTION

This section of the guide examines surface mount assembly processes, proposes thermal profile limits to these processes, and establishes a standard preconditioning flow which encompasses moisture absorption, thermal stress and chemical environments typical in the variety of surface mount assembly methods currently in use. Moisture absorption/desorption characteristics are reported and cracking danger levels are assigned to products identified as crack susceptible by Intel. A discussion of baking to reduce package moisture level, and its potential effect on lead finish solderability is described. In addition, drying, shipping, and storage procedures are described to handle plastic surface mount component (PSMC) packages, which are susceptible to cracking in user's surface mount manufacturing processes within the limits described.

PACKAGE CRACK SUSCEPTIBILITY

There are a number of technical issues that need to be comprehended regarding maintenance of package integrity during board level assembly processing using PSMC. In particular, the phenomenon of moisture induced package cracking during high temperature reflow soldering has been identified. Surface mount assembly subjects the component body to high thermal exposure (215°C–260°C), and chemicals from solder fluxes and cleaning fluids during users' board mount assembly. In through-hole technology the board assembly process uses wave soldering which primarily heats the component leads. The printed circuit board acts as a barrier protecting the DIP package body from solder heat and flux exposure. In order to assure PSMC package integrity through the surface mount process, precautions must be taken by both supplier and user to minimize the effects of reflow solder stress on the component. Plastic molding compounds used for integrated circuit encapsulation are hydroscopic and absorb moisture to a level dependent on storage environment. Moisture can vaporize during rapid heating in the solder reflow process, generating pressure at metal to plastic interfaces in the package. Further stress is applied due to thermal expansion mismatch between the plastic encapsulant and the metal lead frame. This can lead to loss of encapsulant adhesion to the die and the lead frame followed by swelling and finally cracking of the plastic, as illustrated in Figure 6-18. Cracks can propagate either through the body of the plastic or along the lead frame (delamination). Subsequent high temperature exposure and moisture in the package could drive the transport of ionic contaminants through these openings to the die surface increasing the potential for circuit failure due to corrosion.

It should be noted that the phenomenon relates only to risk associated with direct exposure of components to reflow solder process stresses. No loss of package integrity is expected for socketed parts or for through-hole mounted components *not subjected to solder reflow environment*. No current data exists to indicate negative long term effects on reliability of PSMC when package integrity is maintained through surface mount processing. The effect of moisture in these packages and the critical moisture content which will result in cracking failures is a complex function of several package design and material property variables. These include: silicon die size, encapsulant thickness, encapsulant yield strength, encapsulant adhesive strength and thermal expansion properties of materials used in the package. Stress levels imposed by user assembly processes are also obvious determinants of cracking probability. Intel has evaluated PSMC crack jeopardy for its current portfolio. Package moisture level has been measured as a function of temperature and relative humidity. Critical moisture level limits to avoid cracking have been determined and products susceptible to cracking have been identified. Intel is implementing procedures to assure that these products are delivered to users so that packages will not crack during user solder reflow processing. The user must take responsibility during storage, board mount assembly and board rework to avoid package over exposure to moisture by following precautions recommended in this paper. These steps are necessary to assure package integrity is maintained throughout the surface mount process. Intel has developed a reliability "preconditioning" stress qualification sequence which emulates surface mount assembly processing. The effect of these preconditioning stresses and their impact on package performance is not yet fully quantified, however this method is proposed for the purpose of emulating actual process conditions before reliability qualification testing. Users have developed a variety of SMT process flows resulting in the need for a standardized, industry accepted preconditioning flow. This will require a joint effort by IC suppliers and users to define a limiting envelope for worst case process conditions which incorporate the design and material limitations of today's plastic components.



CRACK GENERATION DURING SOLDER

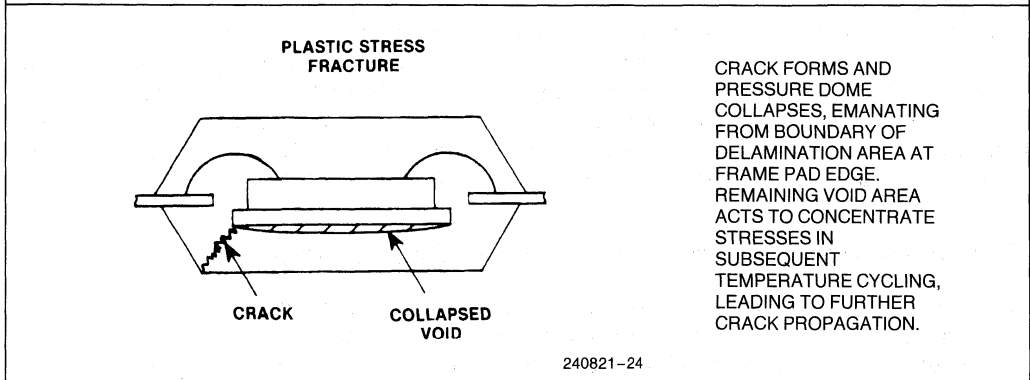
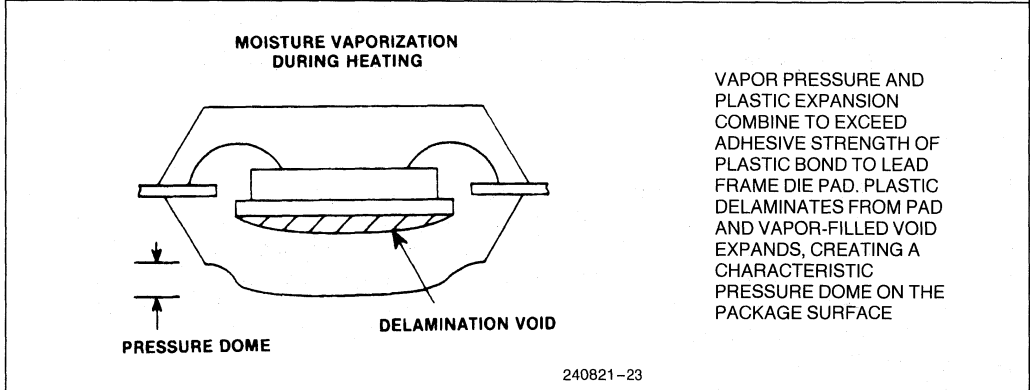


Figure 6-18. Package Crack Mechanism

Surface Mount Assembly Processes

Traditional insertion (through-hole) assembly technology involves relatively few process steps and limits the exposure of components to harsh processing environments. Modern surface mount assembly can be very complex, especially if mixed technologies (surface mount and insertion) are used on the same board. Furthermore, the components are fully immersed in the solder heating media (vapor phase or infrared reflow) in surface mount processes whereas solder heat during solder dip (or wave solder) is applied only to leads of insertion mount packages. Component exposure in both vapor phase and wave solder process environments is illustrated in Figure 6-19.

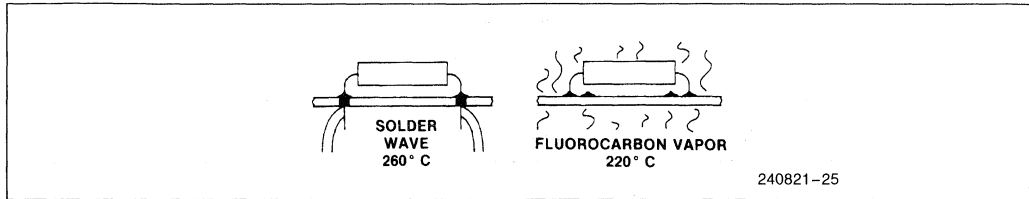


Figure 6-19. Component Exposure to Wave Solder and Vapor Phase Environments

Solder Process

Numerous solder processes are used in attaching components to boards. These range from manual soldering of individual leads with a soldering iron to high volume mass bonding techniques. The two most popular production methods are: vapor phase soldering (VPS) and infrared reflow soldering (IR). *Vapor Phase* soldering uses the latent heat of condensation of a vapor to provide heat for soldering. This latent heat is transferred to the component as the vapor of the inert liquid condenses on the component. The VPS temperature reaches its maximum possible value at the fluid boiling point (219°C). The maximum heating rate of the component on the board occurs when it is initially immersed in the primary vapor, hence control of heating rate for any part is limited to preheating the part before immersion in the primary vapor zone. IR solder reflow processing uses radiant heating to provide heat for soldering. IR panels heat the board traveling on the conveyor from top and/or bottom. A gradual heating of the printed circuit board which is necessary to drive off the volatile constituents of the solder paste assures a controlled heating rate. After an appropriate preheat time, the assembly is raised to the reflow temperature for soldering and then cooled.

Thermal Shock on Components (Vapor Phase versus IR)

Rapid heating and cooling rates also cause thermal shock if there is insufficient time for the center and surface of components to reach the same temperature. Surface temperature, being higher than the internal body temperatures during heating, results in a temperature differential which generates thermo-mechanical stress. The degree of thermal shock on components is higher in VPS than in IR. The IR soldering profile is usually designed to heat the components at a rate of 2°C–6°C per second. Only a limited control can be exerted on the heating rate of components and boards in VPS. The maximum heating rate during VPS is typically much higher (up to 25°C/second). Such high rates of temperature increase can damage PSMC which can crack due to the internal moisture vaporization mechanism described earlier in this Appendix.

Intel has determined guidelines for reflow soldering and post solder reflow component rework which if followed will minimize thermal shock to packages and meet users' solder reflow requirements.

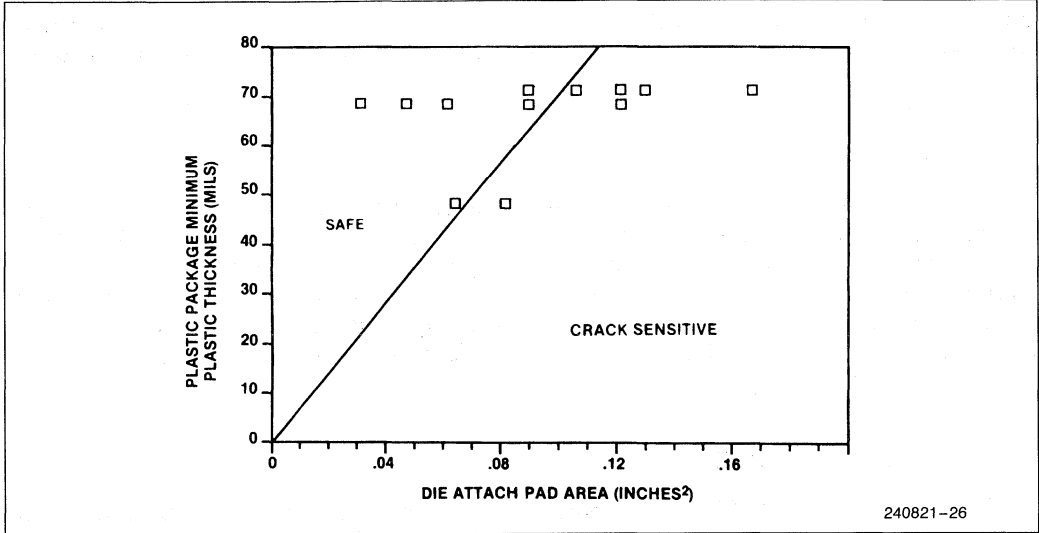
Solder Fluxes

Flux used in solder paste or in board pre-tinning processes is a major source of ionic contamination which can corrode IC chip metallization if transported to the chip surface. Those fluxes containing hydrochloric acid or other halogen compounds should be avoided. Special cleaning methods to assure complete removal of all flux residues should be implemented where use of these materials is selected or required. Highly active fluxes such as organic acid (OA) types should be avoided. RMA or lower activity fluxes should be used if consistent with process yield and solder joint quality objectives.

PSMC Package Cracking

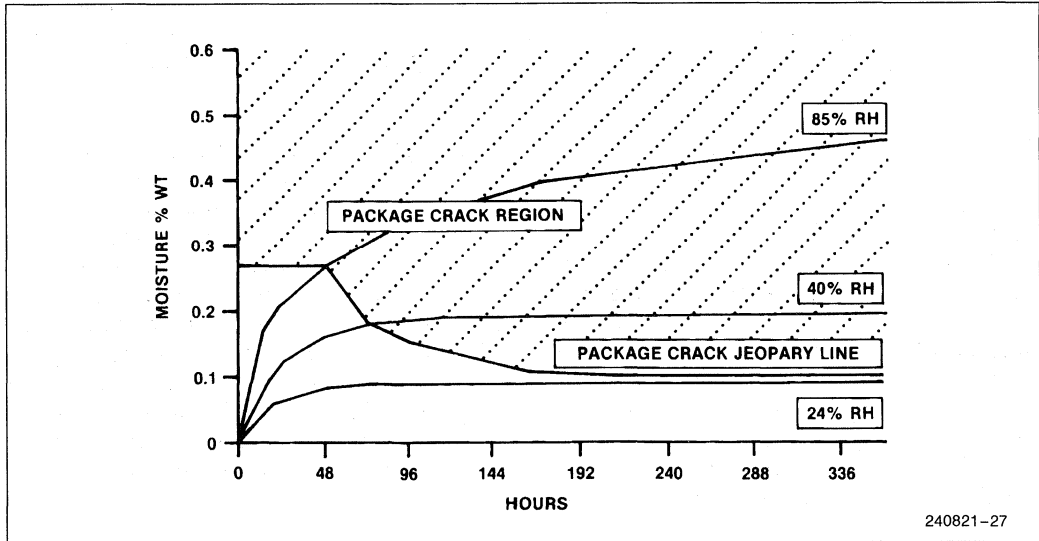
Intel has evaluated its PSMC product portfolio for susceptibility to package cracking during solder reflow processing by subjecting samples to preconditioning stresses which include moisture saturation in 85% RH/85°C for 168 hours, and solder reflow environment exposure. Package saturation in 85% RH was chosen to simulate worst case storage humidity in customers' warehouses, and 85°C is used to accelerate the moisture diffusion rate into the package. The results of this evaluation are described in Figure 6-20 and show that package crack susceptibility is dependent on the die attach pad dimensions and the thickness of plastic between die attach pad and nearest external surface.

A study of package absorption/desorption characteristics has been performed to understand the affect of package moisture content on package crack susceptibility. The resulting data from this experiment are plotted in Figure 6-21. This figure shows the absorption curves for the three humidity levels at 85°C. It also illustrates a "crack jeopardy" line. At any moisture level above the crack jeopardy line, the 68L package that was studied has the potential to generate internal package cracks during vapor phase reflow. in the moisture desorption study, units previously saturated at the humidity levels of 24%, 40% and 85% were baked in an oven at 125°C for a total of 168 hours. The units were removed from the oven, weighed, exposed to VPS solder reflow environment and analyzed for package cracks. Figure 6-22 shows the desorption curves as a function of drying time. This plot also has a "crack jeopardy" line. At any moisture level above this line, the 68L package that was studied has the potential to develop internal cracks during a vapor phase reflow operation. Whereas, at conditions below the line, cracks are not expected to form.



240821-26

Figure 6-20. Crack Sensitive Packages: Package Die Attach Pad Area versus Package Minimum Plastic Thickness



240821-27

Figure 6-21. Crack Generation during Vapor Phase Soldering versus Moisture Absorption: 68-Lead PLCC @85°C

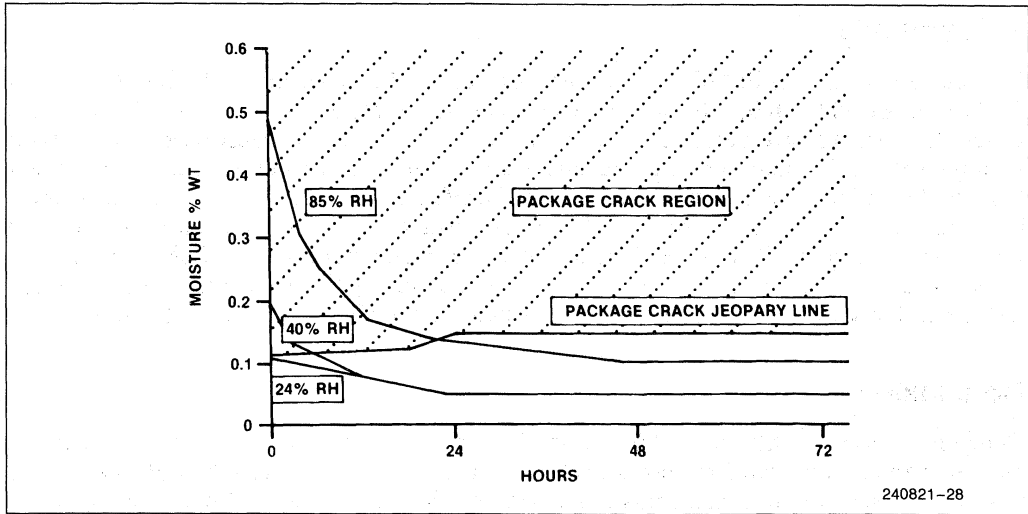


Figure 6-22. Crack Generation during Vapor Phase Soldering Moisture Desorption from Saturation: 68-Lead PLCC @ 125°C

Preconditioning Flow

In order to assure that SMT process stress is comprehended in component reliability evaluations, Intel has established the following product qualification preconditioning flow as shown in Figure 6-23 to which all surface mountable plastic products will be subjected prior to standard component reliability stressing. User assembly processes not comprehended by the preconditioning flow should be discussed with Intel to verify package integrity of Intel PSMC in these applications.

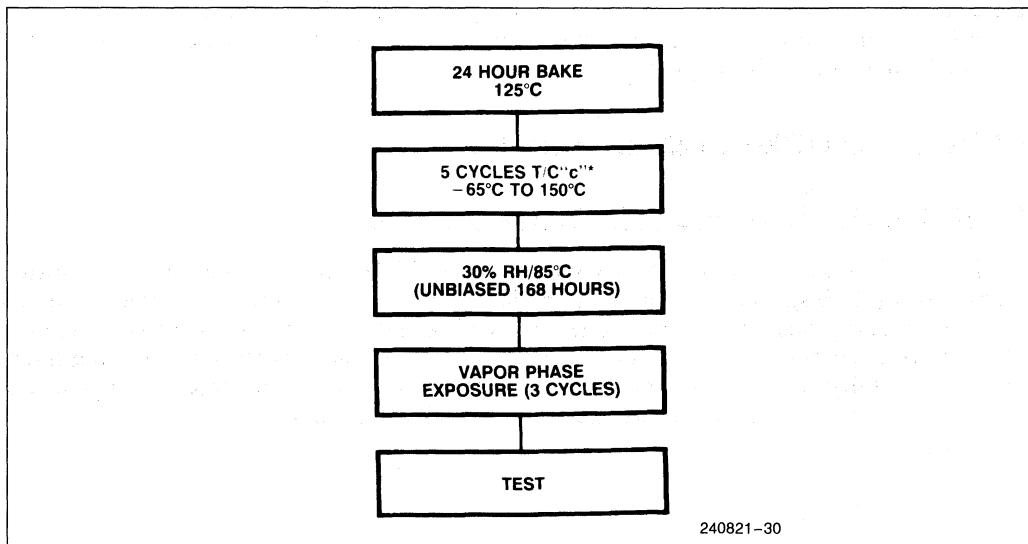


Figure 6-23. Intel® Preconditioning Flow for Surface Mount Packages

Solderability

Intel currently supplies PSMC with copper lead frames and solder finished leads. A potential for lead finish solderability degradation can occur due to formation of Cu_6Sn_5 intermetallic which does not dissolve during the solder reflow cycle. In order to meet users' solderability requirements the formation of intermetallic must be minimized. Intel has performed evaluations to determine solderability degradation of PSMC after burn-in and baking (necessary to drive out package moisture prior to sealing crack sensitive products in moisture barrier bags). Based on the solderability work done at Intel it is recommended that PSMC product be baked at high temperature (125°C) no more than one time by the user. Intel monitors outgoing solderability to assure that product meets user's solderability requirements on every lot.

Conclusion

Component susceptibility to cracking in SMT solder reflow is a function of die and package geometry and is aggravated by moisture absorption in the plastic encapsulant. Package integrity of crack susceptible components can be assured through user assembly if absorbed moisture is kept below critical levels and surface mount process thermal limits are observed. Maximum temperature profile envelopes were recommended for these solder processes to minimize crack jeopardy due to thermal stresses. A standard "preconditioning" flow was devised to simulate SMT processing stresses on component packages prior to reliability qualification stressing. Moisture absorption and desorption characteristics of these sensitive packages have been characterized and moisture concentrations (% by weight) sufficient to induce cracking were determined. When these same packages were dried to below the crack danger level, no cracking was detected after preconditioning (without humidity soak). Crack susceptible components can maintain package integrity during use if they are dried and maintained below critical moisture weight percent levels. Intel will bake these packages dry and seal them in bags with desiccant before shipping. Recommended shelf life, storage conditions, redrying and handling procedures were also described. The user must limit exposure of crack susceptible components to environmental moisture during SMT assembly and rework processing in order to keep absorbed moisture below Intel recommended limits and assure package integrity is maintained through the assembly process.

CONFIGURATIONS AND MATERIALS

Guidelines for Handling Units in Desiccant Pack

Intel will ship plastic surface mount components (PSMC's) in a dry state inside moisture barrier bags (MBB's). The following information is intended to describe the appearance and handling of components shipped in desiccant packing and the materials involved. The handling information applies *only* to those devices subjected to SMT processes. Handling information covers dry component storage life, manufacturing floor life (of exposed components), rebagging information and guidelines for rebaking units if necessary.

PACKING MATERIALS

PSMC's packed in tubes, tape and reel or trays will be shipped in desiccant packing. Each shipping medium will contain units that have been baked dry (24 hours at 125°C) and are enclosed in sealed MBB's with desiccant pouches.

- **Shipping Box.** The #3 shipping box will be the same in appearance as Intel's current shipping box, but the barcode label will indicate that desiccant packed material is included (see Figure 6-24). This label will indicate the seal date of the enclosed MBB and, thereby, the remaining shelf life. Quantities of units shipped per box will also differ to accommodate the additional packing materials for shipments in tubes. Table 6-3 outlines the new tube quantities per box for desiccant packed devices. For details on tube, tray and tape and reel shipments, please see the following sections.

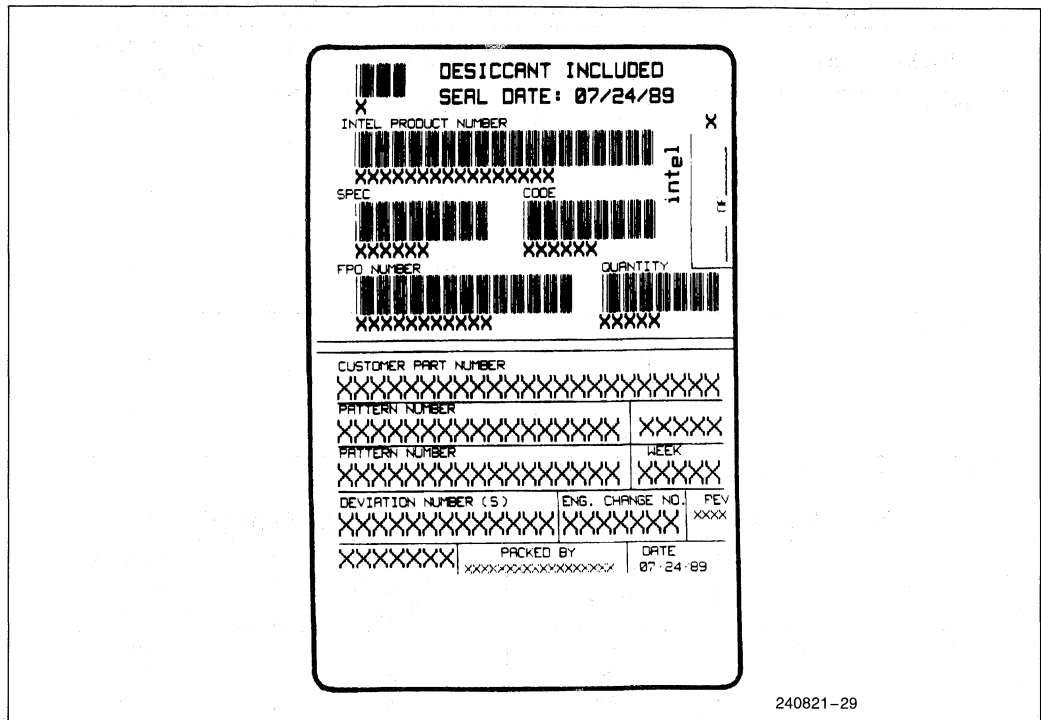


Figure 6-24. Desiccant Barcode Label

- **Moisture Barrier Bag (MBB).** Inside the shipping box is a moisture barrier bag or MBB containing components. The three-ply bag is strong, ESD-safe, and allows **minimal** moisture transmission. It has been sealed at the factory and should be handled carefully to avoid any puncturing or tearing of the materials.

A "Warning Label" (Figure 6-25) will be on the bag, outlining precautions that should be taken with desiccant packed units, and a Desiccant Barcode label.

This bag is intended to protect the enclosed devices from moisture exposure and should not be opened until the devices are ready to be board mounted. The “Supporting Technical Information” section of this document provides information on technical aspects of the bag and characterization information. The “Materials” appendix, following the handling diagrams, outlines basic MBB characteristics.

- **Desiccant.** Each MBB will contain up to three pouches of silica gel desiccant enclosed to absorb moisture that may be present in the bag. The Humidity Indicator card (Figure 6-26) should be used as the primary method to determine whether the enclosed parts have absorbed excessive moisture.

Regardless of the remaining shelf life of the enclosed units, the desiccant should be discarded after opening the sealed MBB. The desiccant should not be baked and is not reusable.

Table 6-3. Quantity Requirements for Desiccant Bags (Tubes)

Package Type	Lead Count	Bag Part #	Quantity of Tubes per Bag
PLCC	20 S	0825	56
	28 S	0825	42
	28 R	0825	56
	32 R	0825	42
	44 S	0825	28
	52 S	0919	60
	68 S	0919	48
	84 S	0919	36
PQFP (Fine-Pitch)	84	0919	16
	100	0919	12
	132	0919	10
	164	0919	8
	196	0919	6

Reels: For PLCC and PQFP in tape and reel, use one (1) reel per bag.

Table 6-4. Quantity Requirements for Desiccant Bags (Trays)

Package Type	Lead Count	# Full Product Trays	Standard Increment (Units/Box)
PQFP (Fine-Pitch)	52	4	420
	68	4	312
	84	4	240
	100	4	220
	132	5	180
	164	5	120
	196	5	105
	244	5	60
TSOP	32	5	360

NOTE:
For kitted products, refer to the S-spec for the standard increment quantity.

**Table 6.5. Number of Desiccant Pouches
per Moisture Barrier Bag**

Type of Shipment	Number of Pouches
PLCC Tubes-Full Length	3
PLCC Tubes-Half Length	2
PQFP Tubes	2
Trays	2
Tape and Reel	3

- Humidity Indicator Card (HIC).** Along with the desiccant pouches, each MBB will contain a humidity indicator card (HIC). This card is a military standard moisture indicator and is included to show the user the approximate relative humidity level within the bag. A representation of the HIC is shown in Figure 6-26. If the 20% dot on the card is *pink* and the 30% dot is *not blue*, the components have been exposed to moisture *beyond the recommended limits for use in an SMT process*. If this should happen, *in order to use these units “safely” in a surface mount application, units need to be baked dry* (see “Rebaking” section). The HIC is reversible and can be reused. Recommendations to avoid expiration of the HIC and the need to rebake units are included in the “Incoming Handling”, “Shelf Life” and “Floor Life” sections.
- Labels.** Labels relevant to this process are the Desiccant Barcode label and the “Warning” label mentioned in the section on MBB’s. The “Desiccant Barcode” label (Figure 6-24) contains the date that the bag was sealed (MM/DD/YY) and is attached to the outside of the box and on the MBB itself. The remaining storage life of the units in the bag is determined from this date. All components are guaranteed 12 months of shelf life starting from the seal date on this label (see following “Shelf Life” section).

The “Warning” label (Figure 6-25) is attached to the outside of the MBB and outlines precautions that must be taken when handling desiccant packed units if they are to be kept dry.

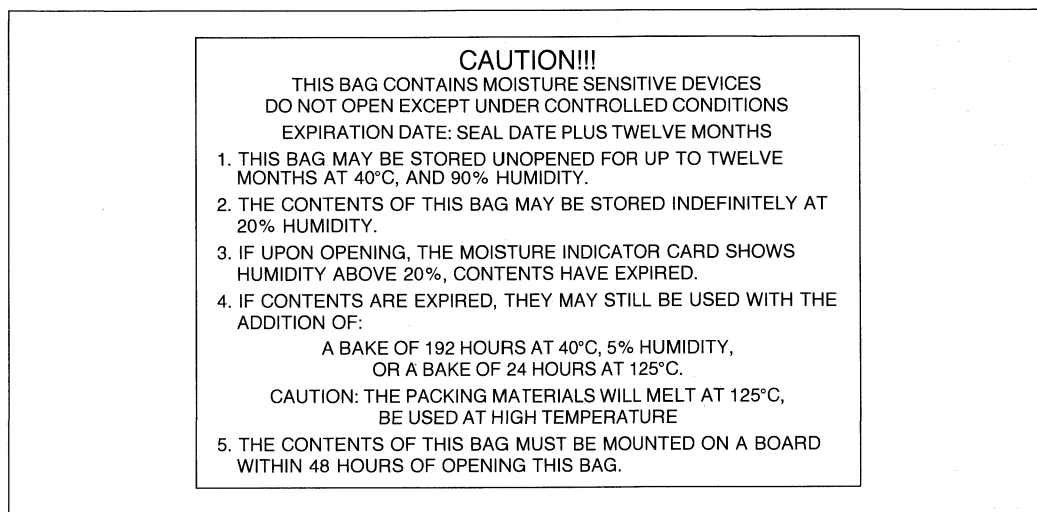


Figure 6-25. “Warning” Label

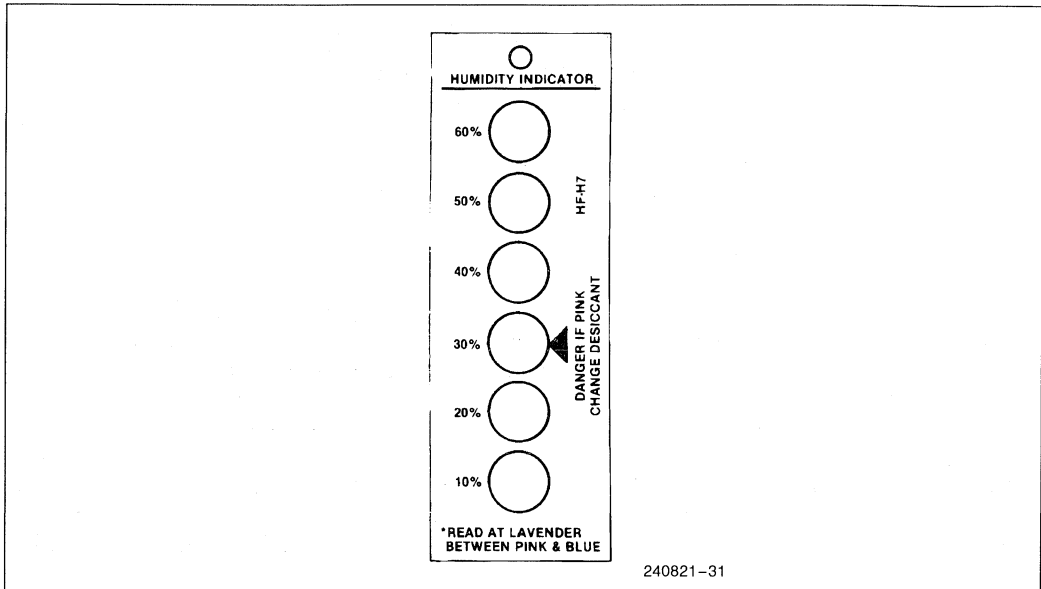


Figure 6-26. Humidity Indicator Card

PACKING OF SHIPMENTS

- **Tubes.** Units shipped in tubes will be packed with an additional precaution. Antistatic foam will be used to protect the bag from the sharp edges of the tubes and tacks. Otherwise, the units shipped in tubes will be packed with materials as indicated in Figures 6-27 through 6-31.
- **Trays.** Units shipped in injection-molded trays will also be packed with additional precaution. Antistatic foam lids will enclose the trays to protect the bag from the sharp edges of the trays. Trays will be packed with materials as indicated in Figures 6-32 through 6-34.
- **Tape and Reel.** Units shipped in tape and reel are packed as indicated in Figures 6-35 through 6-37.

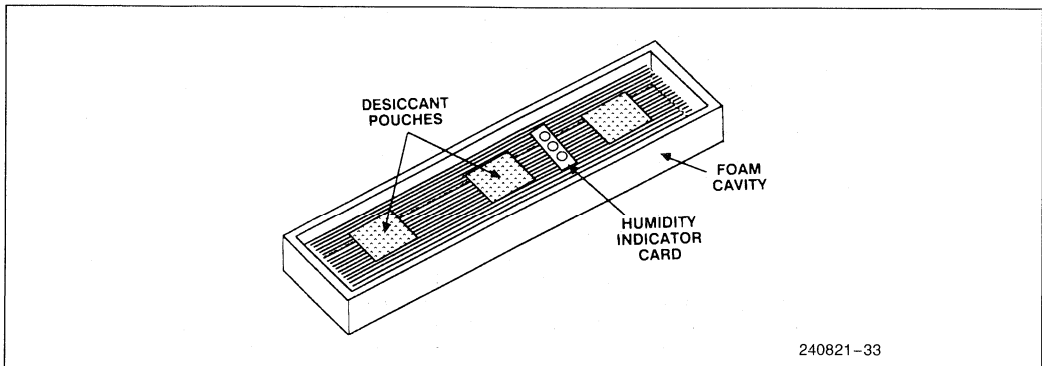
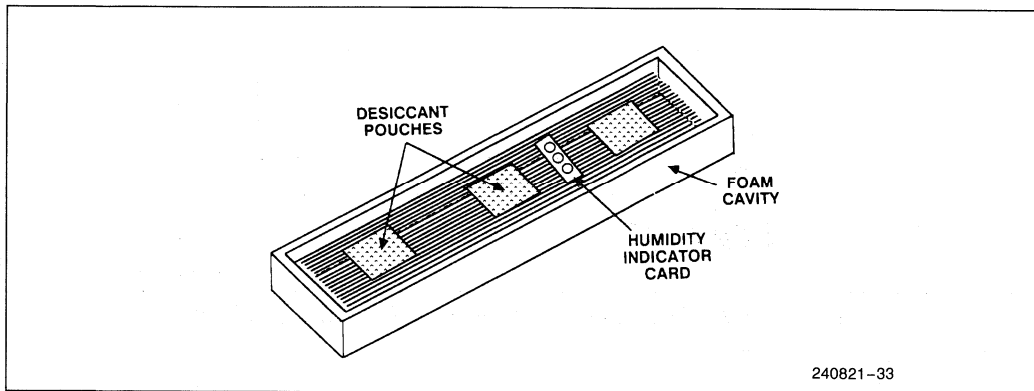
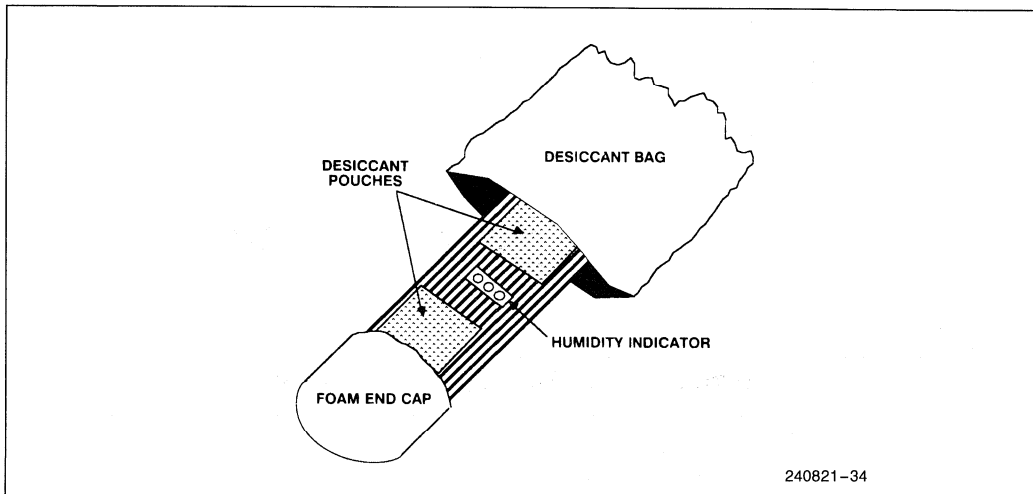


Figure 6-27. Bag Packing for PLCC Full or Half Length Tubes



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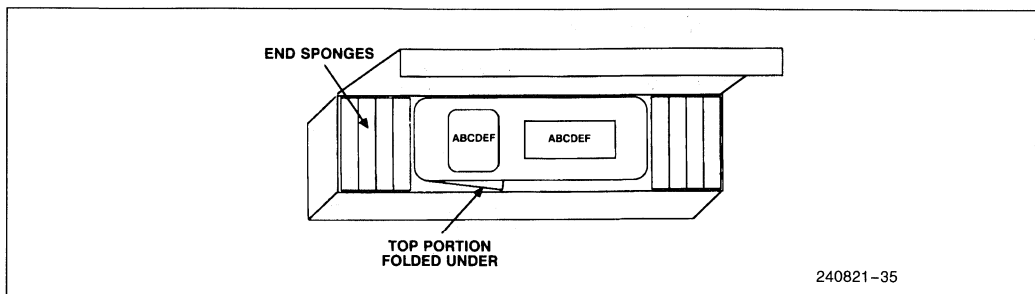
Figure 6-28. Box Packing for PLCC Tubes



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Figure 6-29. Bag Packing for PQFP Tubes



240821-35

Figure 6-30. Box Packing for PQFP Tubes

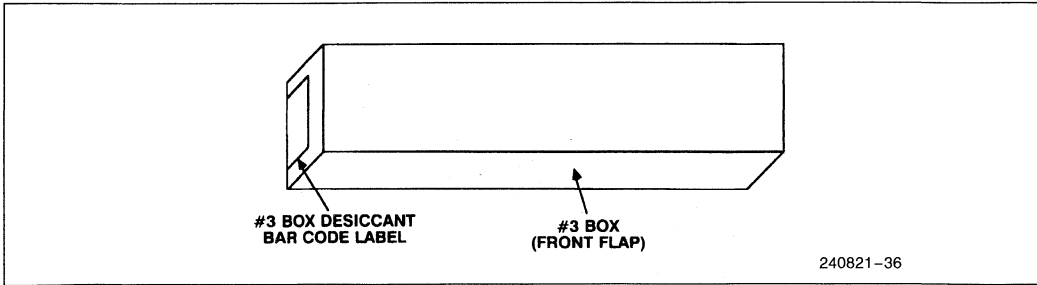


Figure 6-31. Placement of Label on #3 Shipping Box

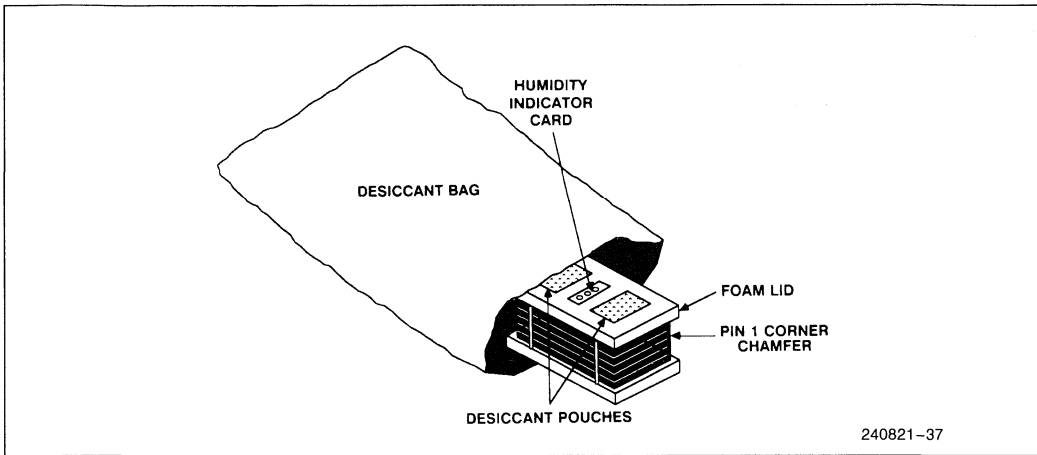


Figure 6-32. Bag Packing for Jedec Trays

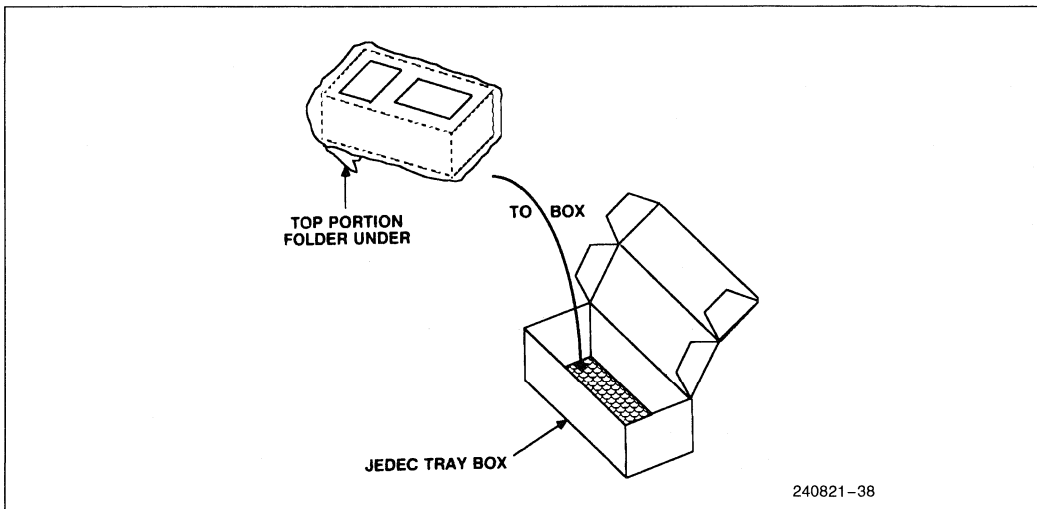
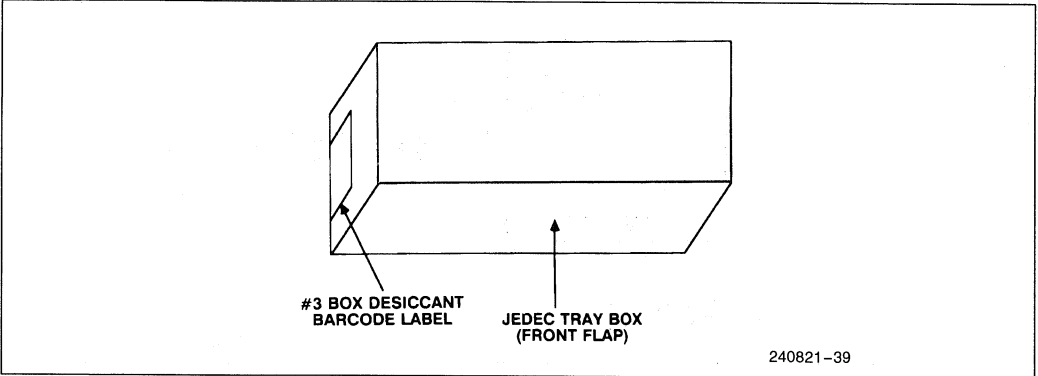
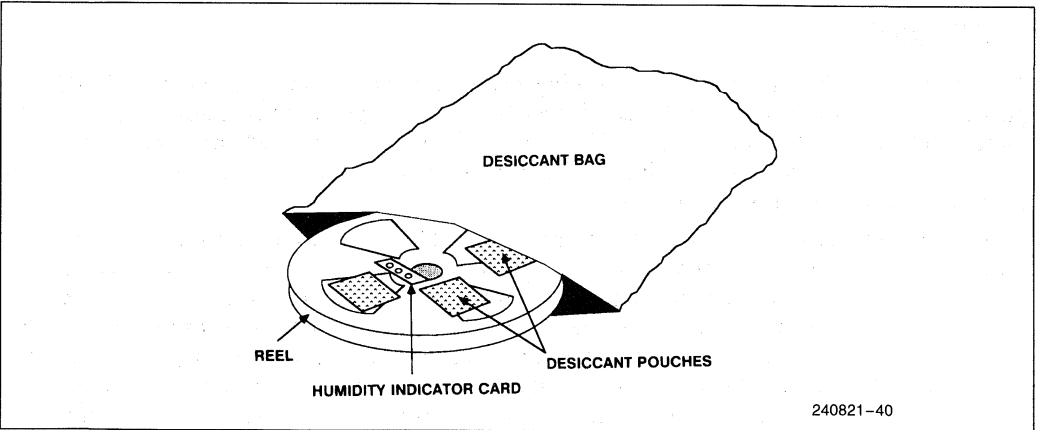


Figure 6-33. Box Packing for Jedec Trays



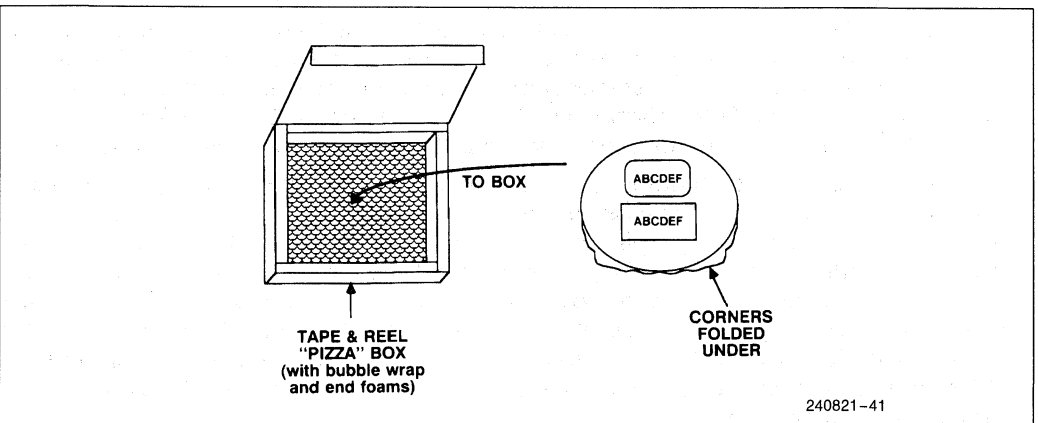
240821-39

Figure 6-34. Placement of Label on Jedec Tray Box



240821-40

Figure 6-35. Bag Packing for Tape and Reel



240821-41

Figure 6-36. Box Packing for Tape and Reel

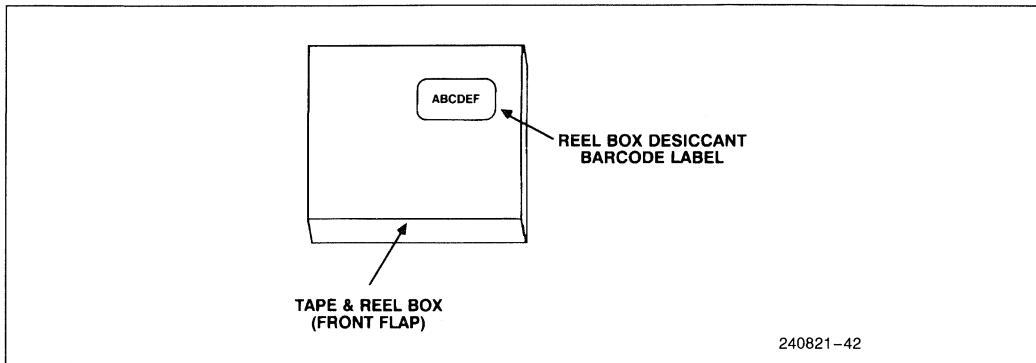


Figure 6-37. Placement of Desiccant Included Label on Tape and Reel Box

HANDLING

The following information details handling procedures that should be used with PSMC's packed in desiccant bags and intended for surface mount applications. Following these handling guidelines will ensure that PSMC's maintain their as-shipped, dry state alleviating package cracking and other possible moisture-related, stress-induced concerns that may be associated with the surface mount process.

- **Incoming Inspection.** Upon receipt, shipments should be inspected for a seal date within the last six months. Bag integrity should also be verified. There should not be holes, gouges, tears, or punctures of any kind that expose either the contents or an inner layer of the bag. The barcode label can be reviewed for conformance to the purchase order, but the bag should not be opened until the contents are ready to be used (either inspected or board-mounted). Please see the following "Manufacturing Conditions/Floor Life" section for details of allowable exposure times once the devices are removed from the bag or exposed to the ambient.
- **Storage Conditions/Shelf Life.** The customer will receive components in the sealed MBB between 0 and 6 months after the seal date indicated on the Desiccant Barcode label. The sealed bag and enclosed desiccant have been designed to provide a total of 12 months of storage (Intel storage time + customer storage time) from the seal date in an environment as extreme as 40°C and 90% relative humidity. The customer will have at least six months of shelf life available on the components without the need to rebake them before use.

If the worst-case storage conditions (time, temperature, or relative humidity) are exceeded and there is a need to verify whether inventory has been affected, a bag can be opened and the HIC can be checked for expiration. If the HIC has not expired (as indicated in the "Humidity Indicator Card" section), new desiccant can be added and the bag resealed ("Resealing" section follows). If the HIC has expired, the devices should be 1) rebaked and used in manufacturing with the guidelines outlined in the "Rebaking" section, 2) rebaked and resealed in an MBB with fresh desiccant, or 3) rebaked and stored in an environment of $\leq 20\%RH$ before they are used in a surface mount process. Please see "Rebaking" section for additional information.

- **Opening MBB's.** To open a moisture barrier bag when the contents are ready to be used or inspected, simply cut across the top of the bag as close to the seal as possible, being careful not to damage the enclosed materials. By cutting close to the seal, you will allow as much room as possible for resealing possibilities. Once the bag has been opened, please follow guidelines for ambient exposure time in the following section to ensure that devices are maintained below the critical moisture level.
- **Manufacturing Conditions/Floor Life.** Once the barrier bag is opened, the information that Intel currently has available indicates that the components must be surface mounted within 48 hours, based on a manufacturing environment not more extreme than 30°C/60%RH. If the components cannot be used within 48 hours, they should be put into a dry storage environment immediately, or resealed in an MBB with fresh desiccant as soon as possible with the remaining parts and fresh desiccant. In either case, the allowable ambient exposure time must be decreased by the time that the units are out of the barrier bag or dry storage environment. In other words, if the parts are exposed to the ambient for three hours, the remaining available exposure time would be 45 hours. 30°C/60%RH is given as a guideline for typical worst-case conditions and is the environment that was used to evaluate component floor life.

In an environment maintained at 40°C/40%RH (or lower temperature *and/or* relative humidity—neither can be higher than 40°C or 40%RH), components may be exposed to the ambient for *up to 92 hours*. All of the same restrictions for exposure time (outlined above) apply.

In more extreme environments, “safe” ambient exposure time will be less. If your manufacturing floor conditions are more extreme than 30°C/60%RH, please consult your local Field Sales Engineer who has been given information regarding technical contacts within Intel.

Where exposure times and/or ambient conditions are difficult to control, Intel highly recommends dry storage capability (please see following section).

- **In-Process Storage.** Intel *highly recommends* having dry storage capability available for units that will not be used within the allowable exposure time. PSMC's can be stored outside of the barrier bag *indefinitely* if the ambient relative humidity is less than 20%. This applies to both long term and in-process storage. A desiccator with dry nitrogen or air ($\leq 5\%RH$ source) is suggested for such storage. (Please see “Materials” appendix following handling diagrams for more information.)
- **Rebaking.** Units need to be rebaked *if and only if* they have been exposed to excessive moisture as indicated by exceeding the recommended 48 hours of ambient exposure time or by expiration of the HIC (see “HIC” and “Desiccant” sections for instructions on how to determine expiration).

In the event that units need to be rebaked, Intel recommends the guidelines outlined in the following text. If the components are to be rebaked *in the shipping tube, tape and reel and trays*, they need to be baked at 40°C (+5°C/−0°C), $\leq 5\%RH$ for 192 hours. The low temperature bake takes longer to dry the devices sufficiently, but does not cause deformation or other detrimental effects to the shipping containers. Handling concerns introduced by the need to transfer devices to high temperature containers associated with the 125°C bake are, therefore, not an issue. Please note that *all other packing materials* such as the bag, desiccant, humidity indicator card, and cushioning materials must be removed to provide free air or nitrogen circulation and *should not be baked*.

A faster bake of 125°C for 24 hours may be used to dry components if they are removed from shipping tubes, or tape and reel. In this case, *only the high temperature plastic trays or metal containers can be used.*

After the bake, components must be; 1) surface mounted within 48 hours for the 40°C bake and 130 hours for the 125°C bake; 2) sealed in a moisture barrier bag with fresh desiccant; or 3) stored in a desiccator (as described above in “In-Process Storage” section) until used. (For technical details behind exposure time, please see “Supporting Technical Information” section.) All bake times given are the time that the oven is at the required temperature and do not include temperature ramps.

Units may be rebaked as many times as necessary using the *low temperature (40°C) bake.* Units *should not be rebaked more than once* if using the *high temperature (125°C) profile* to ensure that solderability is not degraded beyond acceptable limits during the baking process.

- **Resealing Moisture Barrier Bags.** If there is a need to reseal Moisture Barrier Bags for any reason, Intel recommends the following guidelines to ensure that the bag seal does not allow moisture into the bag. The seal area must not exhibit any separation when subject to load and temperature conditions specified in MIL-B-81705B, Paragraph 4.8.1, and must be impermeable to moisture according to MIL-B-81705B, Paragraph 4.8.2. Intel uses a seal pressure to 60 psi–70 psi, and a seal time of 3–4 seconds at approximately 225°C. Intel has qualified the sealer indicated in “Materials” appendix following handling diagrams. (Please read “Note” following this information.) The integrity of the seal is vital to the storage life of the devices.
- **Process Flow.** Intel ships moisture sensitive PSMC which have been packed following a tightly controlled process. This flow is shown in Figure 6-38.

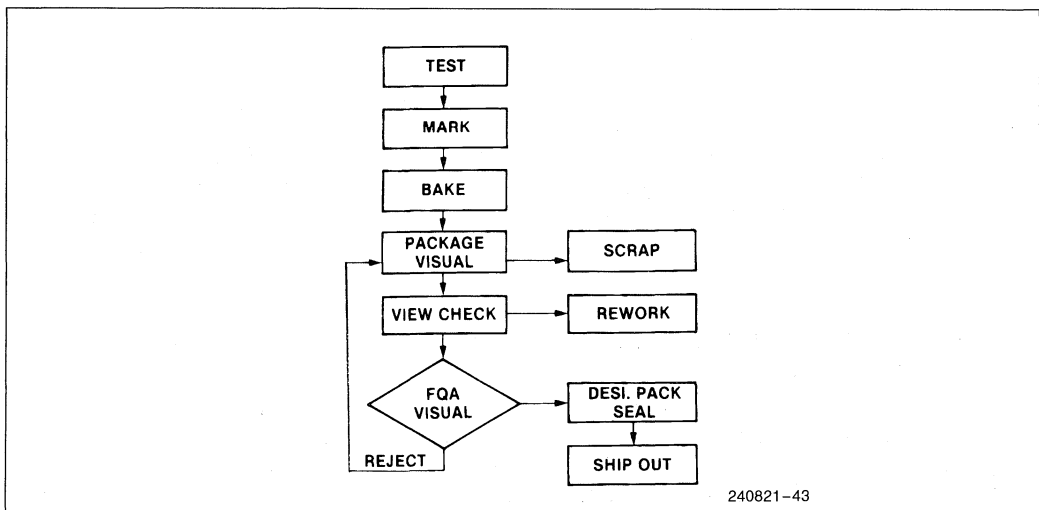


Figure 6-38. PSMC Packaging and Bagging Flow Chart

SUPPORTING TECHNICAL INFORMATION

The phenomenon of moisture induced plastic package cracking during high temperature reflow soldering for surface mount has been discussed by several investigators, including Intel (see Reference 9). Moisture absorbed to a concentration dependent on the storage environment, can vaporize during the rapid heating of the solder reflow process and generate pressure at the metal leadframe-to-plastic interfaces in the package. This, along with the further stress of thermal expansion mismatches between the metal leadframe and plastic encapsulant, can lead to delamination between the die/leadframe and the encapsulant, followed by swelling and cracking of the plastic. Subsequent high temperature exposure and moisture in the package can drive ionic contaminants through these openings to the die surface increasing the potential for device failure due to corrosion. Intel has previously published the saturated moisture level at which package cracking is observed and the safe allowable moisture content for which package cracking jeopardy does not exist (see Reference 9).

Once the cracking jeopardy of *surface mounted* PSMC's was identified, Intel characterized component absorption/desorption rates and saturation limits as a function of temperature and relative humidity. Intel engineers have proposed a model describing the kinetics of PSMC moisture absorption based on this data (see Reference 10). The handling and shelf life guidelines outlined in the first section of this document are based upon the experimental analysis of the desiccant pack materials. The water vapor transmission rate of the moisture barrier bag (MBB), desiccant absorption rate and saturation levels, and maintainable MBB internal relative humidity were all important factors in developing the recommendations given.

Customers using PSMC's in *non-SMT* applications may continue to use PSMC's *without altering their current process flow*. Non-surface mounted PSMC's do not undergo the same temperature excursions and thermal stresses associated with the VPS or IR solder reflow processes and, therefore, do not have the same package crack jeopardy related to them as unprotected PSMC's used in SMT applications.

In previous work (see Reference 9), Intel discussed the reliability "preconditioning" test sequence developed to emulate the surface mount board assembly process prior to qualification testing. As part of that flow, an exposure to 85°C/85%RH was listed with the exception that it was not to be used with "moisture sensitive" product". Following additional experiments, Intel now recommends the revised flow included in Appendix A. This flow indicates stressing "moisture sensitive" units using 85°C/30%RH.

Characterization Data

- **Moisture Absorption.** The moisture absorption curves for the 68-lead PSMC as a function of temperature and percent relative humidity are shown in Figure 6-39. Moisture absorption characteristics of 68-lead PSMC's have been used throughout this work as a worst case behavior limit because of the large die sizes involved. As shown in the curves, temperature is the controlling parameter determining absorption rate in the "short time" view. The saturation limit is a function of both relative humidity and temperature, relative humidity being the major contributor to the final percent weight gain of the components. Earlier work (see Reference 9) reported the allowable safe moisture content to be 0.11% by weight. This line has been overlaid on Figure 6-38. Components absorb this critical amount of moisture rapidly unless they are stored under low humidity conditions, e.g., 20%RH.

- Exposure Times in Different Environments.** The absorption curves for common manufacturing and warehouse environments are shown in Figure 6-40. The allowable safe moisture content line and the intersection of that line with Intel's standard manufacturing floor environment of 30°C/60%RH have been added. At this condition, components absorb 0.11% moisture in 130 hours. Because Intel bakes units, then marks, packs, and ships them to customers, some of this exposure time is expended. The customer will *receive* components which have a minimum of 6 months available shelf life in the customer's warehouse and a 48 hour acceptable exposure time on the customer's factory floor in manufacturing environments of $\leq 30^{\circ}\text{C}/60\%\text{RH}$.

Some customers will require more than 48 hours to complete their board assembly. There are options available to extend the allowable exposure time of PSMCs before SMT reflow processing. Storage in desiccators on the manufacturing floor will extend the working life of units *indefinitely* as long as the time of exposure out of the desiccator is less than a total of 48 hours in an environment no more extreme than 30°C/60%RH. Alternately, *components may be exposed for 92 hours if the manufacturing environment is maintained at 40°C/40% RH or at less severe conditions.*

More severe environments will decrease the acceptable amount of exposure time on the customer factory floor. To assess the impact of other environments, the curves of Figure 6-41 were normalized to the time that the MBB is opened on the customer floor. This family of normalized weight gain versus time curves is provided in Figure 6-41. For instance, the 30°C/60%RH curve crosses the 0.11% weight gain line at 48 hours. From these curves, exposure times in more severe factory environments can be determined.

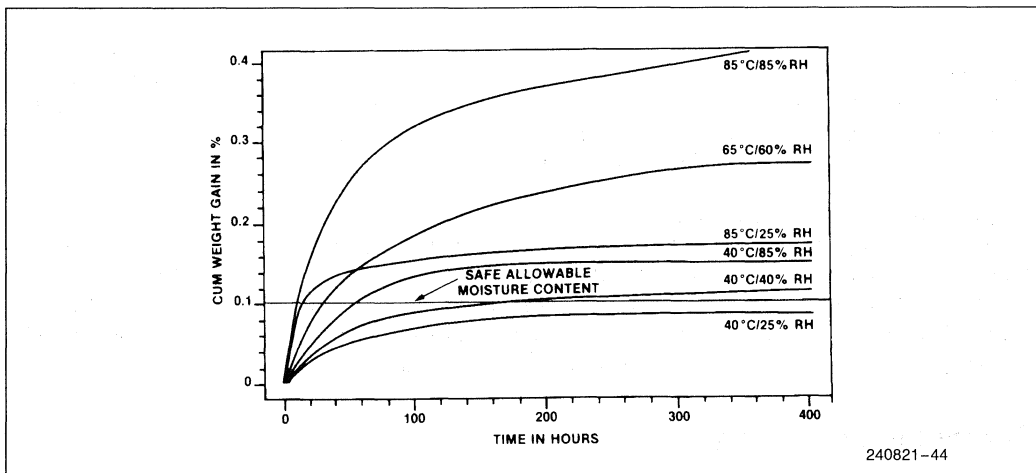


Figure 6-39. Unbagged Component Weight Gain versus T and RH

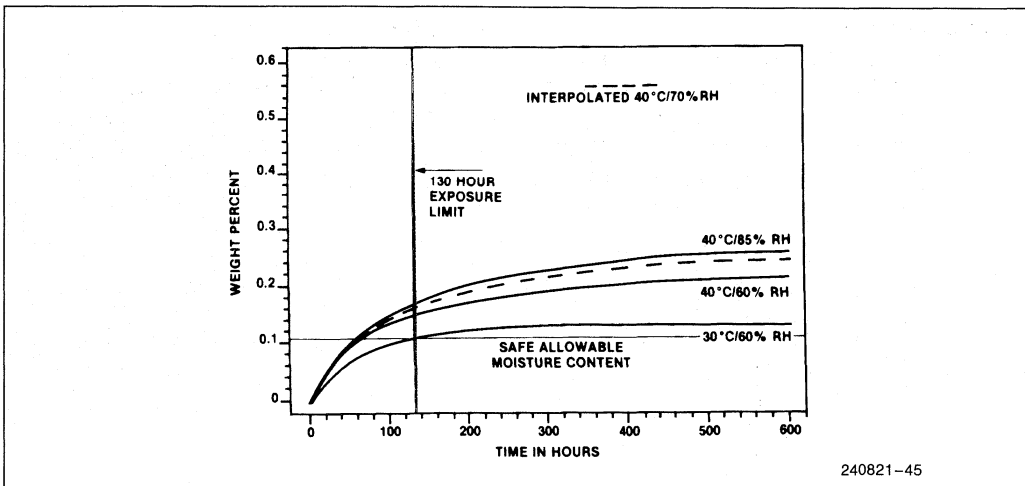


Figure 6-40. Component Weight Gain in Common Manufacturing Environments

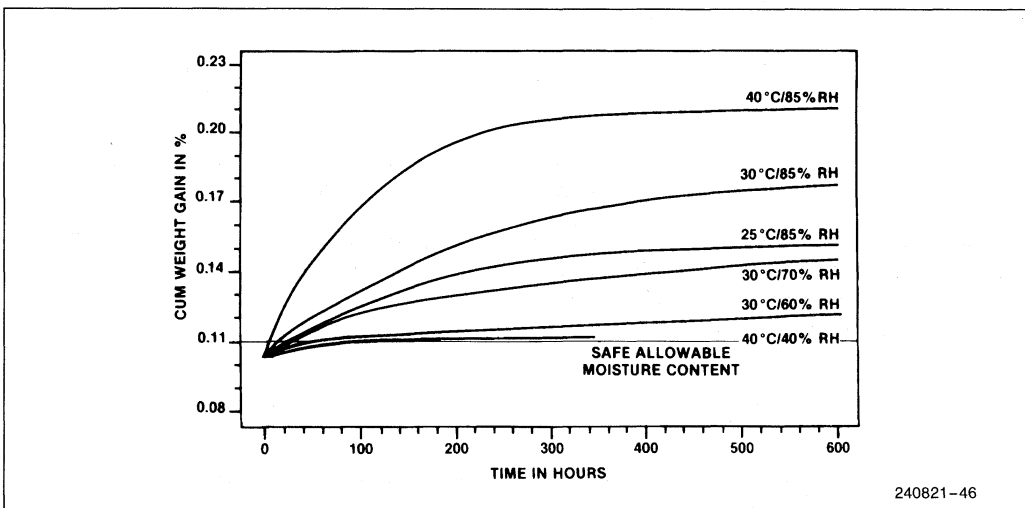


Figure 6-41. Normalized Component Weight Gain

- Desiccant Packing (General).** When components are stored in MBB's with the appropriate amount of silica gel desiccant, it takes much longer for packages to gain the critical moisture content. After 526 hours at 65°C/60%RH, 68-lead PSMC stored in desiccant pack had absorbed 0.008% moisture. The relative humidity inside the bag during this time was <10%RH as measured by the humidity indicator card. The outside storage ambient has relatively little impact on the *PSMC moisture absorption* within the desiccant packing. The respective percent weight gains of bagged components stored at 40°C/25%RH, 40°C/85%RH, and 65°C/60%RH were found to be statistically indistinguishable even after 526 hours of continuous storage. Therefore, the moisture is being absorbed preferentially by the desiccant and the PSMC's see an effective environment of $\leq 10\%RH$.

- Desiccant.** Desiccant moisture absorption as a function of temperature and %RH is displayed in Figure 6-42. The time to saturation is very rapid with increasing relative humidity—within 48 hours at the higher humidities. At 40°C/25%RH, desiccant is still absorbing moisture after 526 hours, however. Figure 6-43 compares bagged desiccant and desiccant in various ambient conditions. The relative humidity inside the sealed MBB is <10%—well below the saturation level of the desiccant.

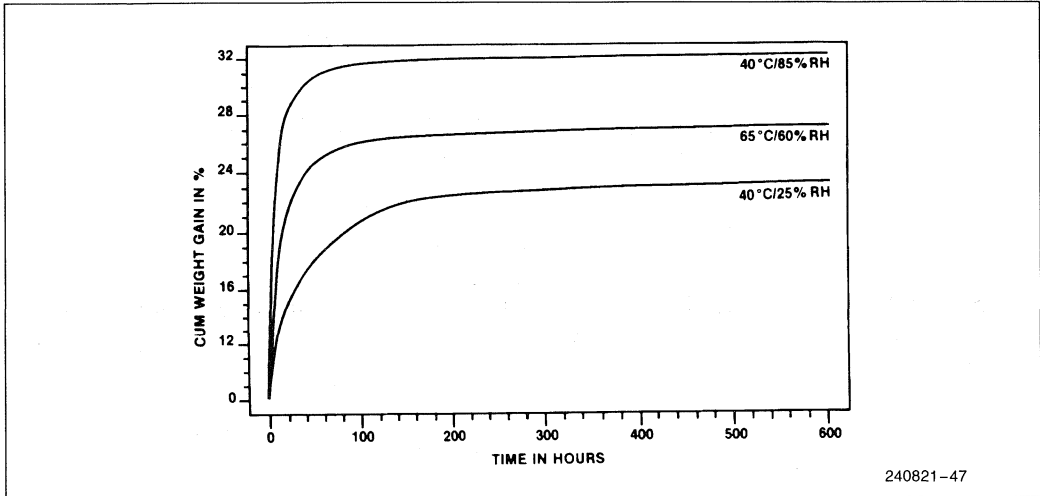


Figure 6-42. Desiccant Absorption versus T and RH

- Moisture Barrier Bag (MBB).** The opaque MBB meets MIL-STD-81705B TYPE I for ESD and mechanical stability. The measured water vapor transmission rate (WVTR) of the bag is better than the MIL-STD requirements for moisture protection. The WVTR = 0.004 gm/100in²/24 hrs as measured at 40°C/85%RH.

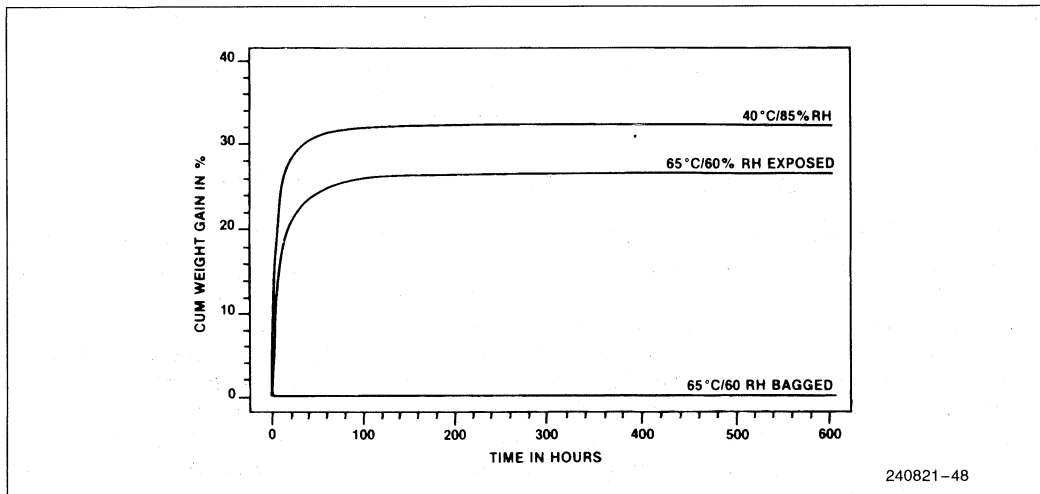


Figure 6-43. Comparison of Bagged Desiccant and Desiccant Exposed to Ambient

- **Amount of Desiccant.** The silica gel desiccant is supplied in 2 unit (50 gm) pouches. The amount of desiccant per MBB is a function of the bag surface area, 0.24 gm/in². See Table 6-3 in the Handling procedures section for specific number of pouches per MBB. The saturation limit for silica gel at 10%RH is 6.8% by weight at 25°C.
- **Shelf Life.** Intel has determined the shelf life of bagged components based upon the bag WVTR, the desiccant absorption rate, and the desiccant saturation limit. The total shelf life (Intel + customer) for bagged components in worst case warehouse conditions of 40°C/90%RH is 12 months.

Rebaking

- **High Temp Bake.** If the HIC indicates that the contents of the MBB have expired, the components can be baked to desorb moisture. Two bake profiles are recommended. The higher temperature bake of 125°C for 24 hours was discussed in the technical paper of the first notification (see Reference 9). This requires that the components be removed from plastic shipping tubes, trays or tape and reel and placed in metal or high temperature plastic containers. Components should be handled carefully to avoid lead coplanarity problems or any other type of damage. After this bake, the units may be exposed to an environment not more extreme than 30°C/60%RH for a maximum of 130 hours.
- **Low Temp Bake.** Intel has also identified a low temperature bake profile. It allows component moisture desorption in the original plastic shipping containers and, thereby, avoids possible damage to component leads that might be introduced through additional handling. The low temperature bake is a 192 hour dwell at 40°C (+5°C, -0°C)/≤5%RH. Figure 6-43 shows the curves for moisture desorption in these conditions. After 192 hours, saturated components will desorb moisture down to a residual moisture content of 0.07% worst case. This will allow a maximum of 48 hours ambient exposure time in environments not more extreme than 30°C/60%RH before the safe allowable moisture content of the package is exceeded. Refer to Figure 6-39, "Component Weight Gain in Common Manufacturing Environments", for the exposure time allowed before the weight percent moisture gain of the package reaches the critical level. The low %RH condition in the oven is critical. Longer bakes are required if the humidity exceeds 5%RH. Note that the temperature of the bake is limited by the thermal stability of the device shipping containers. The shipping containers will not hold dimension at bake temperatures higher than 45°C (40°C +5, -0 as indicated).
- **Solderability Considerations/Number of Rebakes.** Solderability tests performed on PSMC's exposed to either bake cycle are the basis for Intel's recommendations and limits on the number of allowable bake cycles. Work published in the previous technical paper (see Reference 9), established that PSMC's should not be baked more than once by the customer if using the high temperature bake of 125°C for 24 hours. Following this guideline will limit the formation of Cu₆Sn₅ intermetallic and therefore, not promote solderability degradation. The low temperature bake of 40°C for 192 hours does not require this restriction.

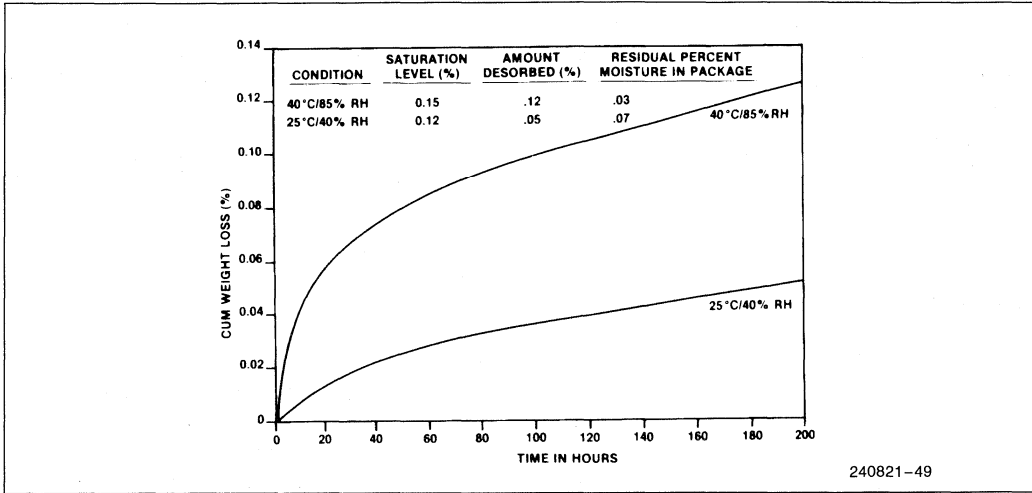


Figure 6-44. Saturated Component Weight Loss at Low Temperature

- Because components are baked in the shipping containers at the 40°C bake—tubes, trays, or tape and reel—possible outgassing products as well as intermetallic formation impact on solderability were evaluated. Figure 6-45 is a “box plot” analysis of solderability measured by coverage of the leads in “number of squares”. There is overlap in the distributions of, 1) the control units stored in metal trays, 2) units stored in plastic shipping containers and, 3) units baked in plastic shipping containers, therefore, there is no statistical difference between the treatments. No difference in solderability was observed after multiple rebakes at low temperature. Based on this data, there is no restriction on the number of times devices can be rebaked at the recommended low temperature before solderability is degraded beyond acceptable limits.

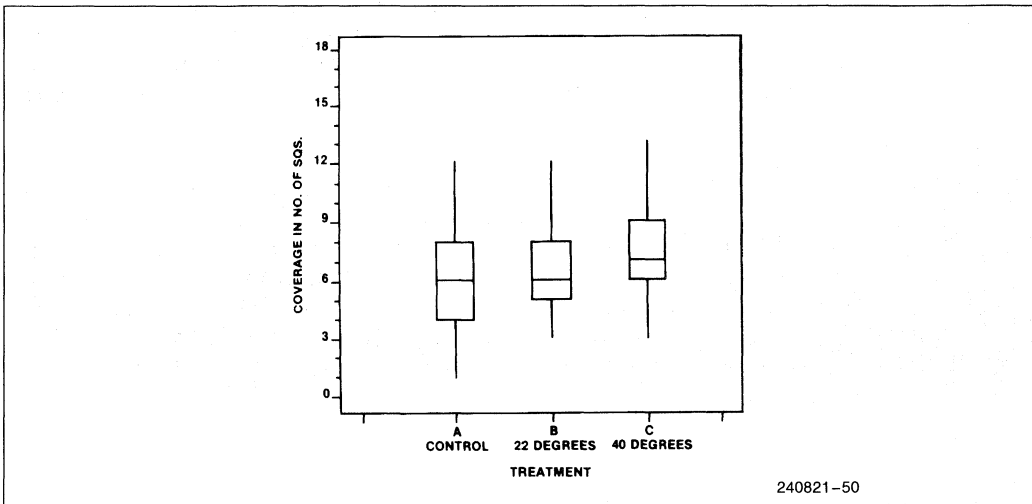


Figure 6-45. Solder Coverage versus Temperature

EVALUATION OF PSMC DEVICES FOR MOISTURE SENSITIVITY

The problem of moisture stress sensitivity and package cracking during surface mount is not unique to any one computer design or manufacturer. A method is needed for evaluating the “moisture sensitivity” of devices supplied by different manufacturers. The method that Intel has developed to determine whether a package/die combination is “moisture sensitive” with respect to package cracking follows. Uniform application of this methodology is one way to evaluate devices from different vendors to determine which devices, if allowed to absorb moisture, have a high probability of cracking during surface mount procedures. Also included is a method which can be used to assess device failure rates in surface mount applications. This can also be useful for comparison purposes and comprehends failure rates due to any kind of surface mount induced, stress-related failure. This method is commensurate with that being proposed by the IPC in IPC-SM-786.

Method for Evaluating Devices for Package Cracking

NOTE:

One product cannot be used to categorize a vendor's entire portfolio as moisture sensitive or not, since package cracking is a function of die paddle area (the area of the lead frame where the die is attached) and minimum package plastic thickness. Each product must be evaluated individually.

- Bake 10 units of each product for 48 hours at 125°C to dry out any absorbed moisture (preferably 5 units from each of 2 date codes).
- Saturate the units by soaking in an unbiased Temperature/Humidity chamber for 168 hours using the following temperature/humidity combinations:
 - Use 85°C/85%RH to simulate behavior under uncontrolled storage conditions.
 - Use 85°C/30%RH to simulate behavior of “dry” units shipped in desiccant pack or units baked prior to surface mount and then exposed to the ambient for the maximum allowable exposure time.
- Run the units through one pass of solder reflow (vapor phase or infrared) within 8 hours of removal from Temperature/Humidity chamber.
- Pot the units, in preparation for cross-sectioning, using an epoxy resin such as Kold-mount (Vernon-Benshoff Co.) or Buehler Epoxide Resin. The units should be placed in the mold with the package edge down rather than with the leads down. Several units can be potted together.
- Cross-section the sample using a diamond saw to cut through the die center. This area has been found to be “worst case”. A cross-section can also be taken at an edge of the die (see attached Figure 6-46) if desired. (X-raying the units prior to potting will aid in determining where to cross-section). Polish to a 6 micron finish.
- Clean the sample using isopropyl alcohol in an ultrasonic cleaner.
- Examine the cross-section at 30X under a stereo microscope to look for package cracks.
- Observations can be classified into three general categories: 1) no visible cracks, 2) short cracks, and 3) long cracks. Any crack which reaches more than two thirds ($\frac{2}{3}$) of the distance to the lead frame or package edge is considered a long crack. This distinction is for comparison purposes only.

Devices which exhibit package cracking after saturation at 85°C/85%RH have an increased probability of cracking during the SMT process if they are surface mounted after storage under uncontrolled conditions. Such devices should be treated as “moisture sensitive” and only used in a “dry” state for SMT applications. This “dry” state can be achieved either by baking the units prior to surface mount or by receiving “dry” devices in desiccant pack from the vendor (as Intel currently provides).

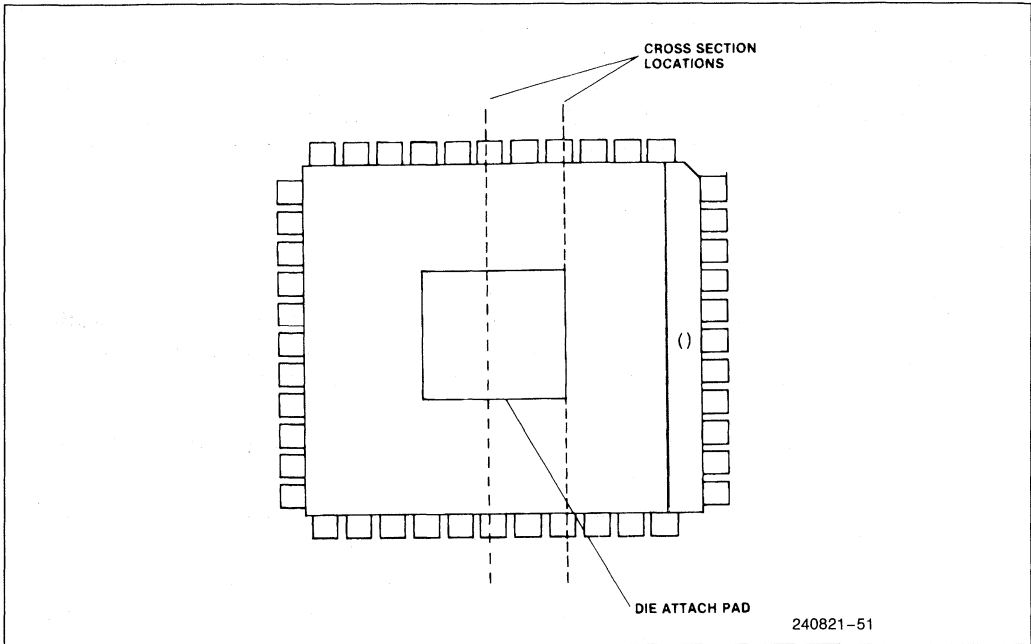


Figure 6-46. Package Crack Analysis Cross Sectioning Locations

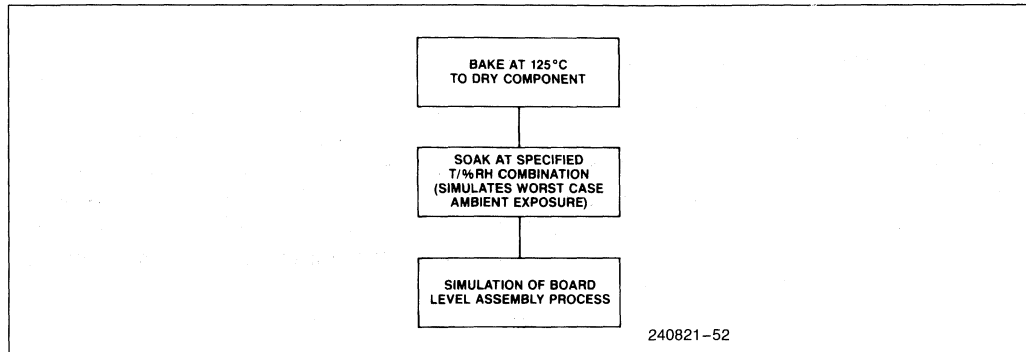
The method outlined above only indicates whether or not a device is susceptible to package cracking. To evaluate surface mount related failure rates over time, it is necessary to stress the units. The following describes a procedure using temperature cycling and THB (temperature/humidity, biased) stressing to evaluate failure rates due to any kind of surface mount-related, stress-induced failure.

Method for Evaluating Device Failure Rates

- The following flow (as shown in Figure 6-47) will determine the failure rate of one product from one vendor. The process should be duplicated for additional vendor/product combinations that need to be assessed.
- Determination of failure rates and resulting comparisons should only be made after analysis of failures has been completed. Invalid failures may result and should not be used in the final failure rate assessment.

- Precondition 154 units per lot from three different lots of the same product (462 units total). This flow simulates the conditions and chemical exposures a device typically sees during board mount and rework as indicated.
- A reduced sample size of 90 units per lot (270) total can also be used. Sample sizes given are based on LTPD charts given in MIL-STD 38510.
- Please note that the preconditioning flow given here is a generic flow.
- Following pre-conditioning, divide each of the three lots in half and subject them to the following stresses:

THB (85°C/85%RH, Biased)		Temp Cycle MIL-STD Condition "B"	
3 lots of 77 units each (45)		3 lots of 77 units each (45)	
Read-out at	168 hours	Read-out at	200 cycles
	500 hours		500 cycles
	1000 hours		1000 cycles



**Figure 6-47. Preconditioning Flow for Surface Mount Packages
(before Temp Cycle and THB Stressing)**

Numbers given in () represent number of units if using reduced sample size.

- All read-outs are electrical read-outs.
- Once again, failures should be analyzed before device failure rates are evaluated.

THB and Temp Cycle failure rates are not easily correlated to field failure rates unlike failures which occur during high temperature lifetesting (burn-in). However, failures which occur during THB and Temp Cycle stressing can indicate a potential problem and should be discussed with the vendor.

VPS/IR SOLDER REFLOW PROCESS RECOMMENDATIONS

Reflow Profiles

A typical infrared reflow temperature-time profile of a PLCC solder joint in an in-line oven is shown in Figure 6-48. A typical vapor phase reflow profile of a PLCC solder joint in a batch oven is shown in Figure 6-49. Table 6-6 lists the important characteristic parameters and

their recommended limits for these profiles. To establish an infrared reflow profile, the conveyor speed and the oven panel temperatures have to be established. To establish a vapor phase profile for batch machines, the elevator speed and board dwell time in the primary zone have to be established.

HEATING RATE

To avoid a thermal shock on sensitive components, their maximum heating rate, also called the maximum ramp rate of the temperature, should be controlled. For infrared reflow, the maximum heating rate can be maintained below 2°C per second in most in-line IR ovens, even though in some ovens, this maximum may occur in zones following the preheat zone. In Figure 6-48, the maximum ramp rate occurs in the preheat zone.

For vapor phase reflow, because of the sharp temperature transition between the primary and the secondary vapor zones, the maximum heating rate cannot be maintained below 2°C per second. With proper elevator or conveyor speed and preheat temperature adjustment, the maximum heating rate can be controlled below 6°C per second.

PEAK TEMPERATURE IN PREHEAT ZONE

During infrared reflow, the boards are preheated in the initial zone of the oven, which is also called the preheat zone. To avoid over-baking the solder paste and exceeding the glass transition temperature of the epoxy in FR-4 boards, the peak temperature in the preheat zone of the boards and the solder paste on the lands should not exceed 125°C in IR ovens. For vapor phase reflow, boards are generally preheated in a separate oven; either a batch convection oven or an in-line infrared oven. In any case, the peak temperature of the boards and the paste during preheat should not exceed 125°C .

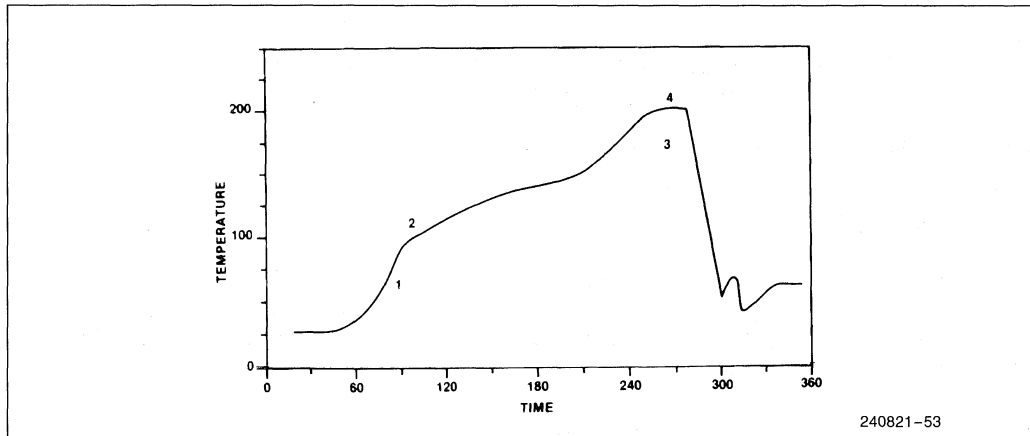


Figure 6-48. A Typical Infrared Reflow Temperature-Time Profile of a PLCC Solder Joint in an In-Line Infrared Oven

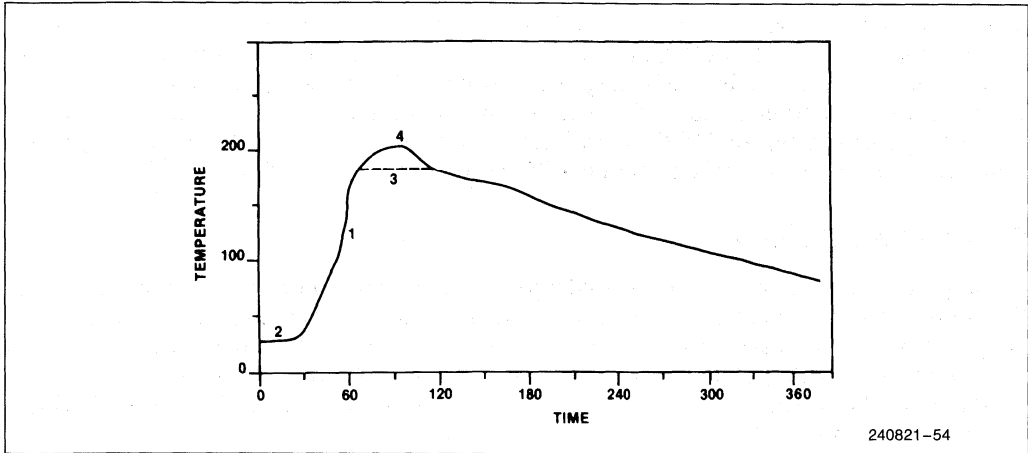


Figure 6-49. A Typical Vapor Phase Reflow Profile for a PLCC Solder Joint in a Batch Vapor Phase Machine

Table 6-6. Table of Limits for Critical Reflow Profile Characteristics

Characteristic # (Figures 6-48 & 6-49)	Characteristic Description	Infrared Reflow	Vapor Phase
1	Maximum Heating Rate	2°C/sec	6°C/sec
2	Peak Temperature in Preheat Zone	125°C	125°C
3	Duration of Time above Melting Point of Solder	Min—10 secs Max—80 secs	Min—10 secs Max—80 secs
4	Peak Reflow Temperature	Min—200°C Max—225°C	Min—205°C Max—220°C

TIME ABOVE SOLDER MELTING POINT

A minimum of 10 seconds and maximum of 80 seconds is recommended for the duration of time that the solder at the joint is above its melting point. The solder should be given sufficient time above its melting point to flow and wet the lands and the leads. However, extended duration above the solder melting temperature will damage the board and sensitive components. Moreover, excessive intermetallic compound formation between the solder and the base metal of the lands and leads will occur which may degrade solderability and solder joint fatigue characteristics.

PEAK REFLOW TEMPERATURES

The peak temperature of the solder joint during reflow should be high enough for adequate flux action and solder flow to obtain good wetting. However, it should not be so high as to cause component and board damage or discoloration. In infrared reflow ovens, the peak reflow temperature is primarily controlled by the panel temperatures in the reflow zone and

secondarily by the conveyor speed. In infrared reflow ovens, the peak temperature of the PSMC should be limited to 225°C. In vapor phase reflow, the peak reflow temperature of the solder joint is determined by the boiling temperature of the primary fluid and the dwell time of the board in the primary zone. The standard primary fluid used for surface mount assemblies has a boiling point of 215°C at sea level. Hence, accounting for elevation changes, the peak temperature of the package during VPS reflow is limited to 220°C.

OTHER CHARACTERISTICS

Cooling rate: The cooling rate of the solder joint after reflow is important because the faster the cooling rate the smaller grain size of the solder. Smaller grain size solder has a higher fatigue resistance. If fans are used to cool the boards after they exit the oven, a cooling rate of 10°C per second at the solder freezing point can be easily achieved. However, if there are no cooling fans, the cooling rate at the solder freezing point is less than 1°C per second. This is illustrated in Figure 6-49.

Duration of time the board temperature is above 150°C: the duration of time the board temperature is above 150°C should also be minimized. Glass-epoxy FR-4 boards can be damaged if kept above 150°C for an extended duration of time because the glass transition temperature of the epoxy is exceeded. This duration should be limited to 2 minutes maximum.

Rework Profiles

Generally, rework of surface mount components is done by using hot air reflow. Hot air is blown on the leads and the solder joints of the part to be reworked and the part is pulled away from the board once the solder on all solder joints is molten.

Figure 6-49 shows a typical temperature-time profile of a lead on a 84-lead PLCC while being reworked using a hot air rework machine. Initially, the leads are preheated with the nozzle some distance away (typically an inch or more) from the package body. Then, the nozzle is lowered to a point just above the package body and the temperature of the leads increases sharply till it reaches a peak. At this point the package is removed from the printed circuit board.

To prevent moisture-related damage in SMT components during removal, perform rework/removal before the 48 hour exposure limit has expired. If this is not possible, the populated boards should be baked at either 125°C for 24 hours or 40°C for 192 hours. *Note: if the exposure time limit has not yet expired, storing the populated boards in a desiccator (<20%RH) until rework/removal is done will eliminate the need for a bake.*

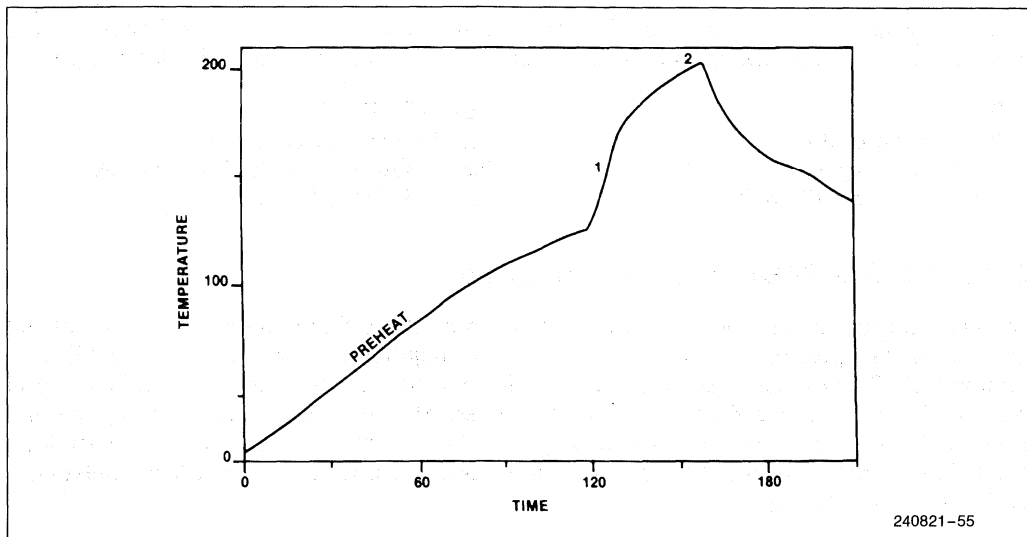


Figure 6-50. A Typical Temperature-Time Profile of a Lead on an 84-Lead PLCC while the Package was being Reworked with a Hot Air Rework Machine

HEATING RATE

The quickest ramp rate in the hot air rework profile occurs when the nozzle is lowered on to the package after preheat. This section is denoted as 1 in Figure 6-50. This temperature ramp rate should be restricted to less than 8°C per second to avoid excessive thermal shock on the package body.

PEAK TEMPERATURE

The peak temperature of the leads during the rework procedure should obviously be greater than the melting point of the solder in the solder joint. However, if the peak temperature is too high there is the possibility to damage the package or the printed board by excessive heat application. For eutectic tin-lead solder, this peak temperature, denoted by 2 Figure 6-50, should be in the range 200°C to 230°C.

OTHER CONSIDERATIONS

Nozzle design is very critical to obtaining an effective rework profile using hot air rework equipment. Generally, the leads on the edges of the package heat up quicker than the leads towards the center. Consequently, the edge leads reach the melting point of the solder before the center leads on each side of the package. The difference in temperature lag between the edge and center leads is greater for larger packages and for poorly designed nozzles can be 20°C. However, with a nozzle that blows more air on the center leads, this temperature can be reduced to less than 5°C.

The following is a list of vendors who supply aluminum tubes suitable for baking PSMC packages in users' processing to remove moisture from packages prior to Solder reflow:

TDA
1924 South East 64th
Portland, Oregon, 97206 U.S.A.
Phone # (503) 775-6791

BELL-CARRY
14913 Gwen Christ Court
Paramount, California 90723 U.S.A.
Phone # (213) 531-2070

SMC BOARD REMOVAL TECHNIQUES

Intel recognizes the need for SMC board removal procedures that maintain the electrical and mechanical integrity of the component leads. The requirement for electrical testability of removed SMCs is driven by the need (1) to confirm device failure as the cause of board-level nonfunctionality, (2) correlate device failure between the customer board assembly site and Intel, and (3) perform electrical testing as part of the failure analysis procedure. Therefore, the following removal procedure has been developed to ensure component lead coplanarity and lead finish integrity.

Recommended Materials for Removal of SMCs

Materials used in the removal of SMCs are as follows:

- PCB with device to be removed
- Pace Craft-100, Air-Vac DRS-21, or equivalent* hot air solder reflow system
- Nozzle for optimized air flow. The nozzle is package dependent.
- Vacuum cup. The vacuum cup should be large enough to cover the center of the device without extending over the leads.
- Tweezers
- Safety glasses
- Pallet to retrieve component once it is removed
- Solder wick or hot air gun/blade

NOTE:

*The above is not an endorsement of any kind nor a warranty of performance of the equipment or company.

BOARD PREPARATION

Many plastic surface mount components and some ceramic chip components are moisture-sensitive. In addition, glass fiber-reinforced PCB materials can be subject to measling and other thermal-/humidity-induced damage.

As discussed in the section on desiccant pack, the package body is not heated by direct impingement of hot air. However, it can reach significant temperatures by radiant and convective heating from proximity to the reflow air nozzle. Therefore, rework procedures should be calibrated to prevent package body temperature from exceeding 200°C.

Moisture-sensitive surface mount components should be dried by a prebake prior to rework to prevent damage to the board and the component. If it is determined that the component for removal is not moisture-sensitive, standard assembly handling and preheat procedures should be followed (see section below on “Removal Procedures”). If the component has been exposed to excessive moisture, it is necessary to dry it by baking the entire assembly at either 125°C for 24 hours or 40°C for 192 hours.

The air flow of the rework nozzle should be calibrated to ensure that leads and solder exceed the reflow temperature of the solder joint. The temperature of the package body should remain below 200°C.

REMOVAL PROCEDURES

The following procedures are recommended for removing SMCs from the PC board:

- Turn on the rework equipment at least 20 minutes before beginning the removal procedure to ensure that the air flow is at the correct temperature. Insert the PCB into the work holder.
- Adjust the work holder so that the device is centered under the hot gas nozzle. Lower the nozzle over the device and align. The alignment of the nozzle to the device is critical to ensure a uniform heating rate of the leads.
- Raise the nozzle and lock it into position. Lower the vacuum cup and check that it is the proper size.
- To reflow the solder, set the timer for the appropriate dwell time for the package type and size, as listed in Table 6-6. Pressure and time can be adjusted to optimize the process, but any modifications for increased throughput should not increase the temperature of the component body above 200°C.

Lower the nozzle until it is 5 mils–10 mils above the shoulder of the leads. This height is crucial: If the nozzle is too high, the heating time must be increased; if positioned too low, the nozzle can cause damage to the leads.

- Using the automatic mode, reflow the solder. Once the air flow has shut off, immediately raise the component from the board. Icicling can be minimized or eliminated by removing the component from the board surface quickly using a smooth upward motion. The direction of removal must be normal to the plane of the board to prevent bridging. Do not twist or tilt the component during the removal process.
- To retrieve the component once it has been removed from the board, use the pallet (Pace safety handle). Turn off the vacuum and let the part drop onto the pallet. The drop distance should not exceed 2 in.

NOTE:

If resistance is felt when lifting the component off the board surface, do not force the part. Re-expose the unit to the heating cycle and then repeat the removal process. If the component still will not separate from the board, terminate the removal procedure. Determine if the component has been adhesively attached to the board. If so, alternate removal procedures—not covered here—will be required for removal.

Table 6-7. Parameters for Component Removal (Based on the Pace Craft-100)

Package Type	Lead Count	T_{lead Center} (°C)	T_{lead Edge} (°C)	Min Time (sec)
PLCC	32	282	277	25 + 5/ -0
	44	291	281	25 + 5/ -0
	68	277	276	35 + 5/ -0
PQFP	100	270	250	35 + 5/ -0
	132	280	250	35 + 5/ -0
	164	280	250	35 + 5/ -0
Cerquad	32	269	271	55 + 5/ -0
	44	289	277	55 + 5/ -0
	68	251	252	60 + 5/ -0

NOTE:

Pace air stream temperature = 350°C

Pace N₂ pressure = 40 psi

REWORK OF LEAD SURFACE MORPHOLOGY AFTER REMOVAL

Intel has found that careful removal of SMCs using the above recommended procedures greatly reduces the need to rework leads. However, if bridging or icicling occurs, Intel recommends the use of solder wick or a hot air gun for rework.

Bridging can be removed by using a solder wick. Holding the solder wick over the bridged leads, bring a fine-tip soldering pencil in contact with the bridged area. When the solder reflows, touch the wick to the molten solder, absorbing the excess.

Icicling can be eliminated by reflowing the solder with a hot air gun ($T > 190^{\circ}\text{C}$). Place the part, leads up, on a heat-resistant horizontal surface. Run the hot air blade or gun across the affected leads, reflowing the solder. Allow the solder to fully resolidify before moving the component. Be sure that the hot air knife does not increase the localized package body temperature above 200°C.

NOTE:

This procedure was developed on a Pace Craft-100 rework station. Critical configuration requirements include a hot air source capable of maintaining 350°C, a nozzle design that evenly distributes air flow to all four sides of the package, and a timer. *Intel recommends that customers calibrate their removal systems to achieve commensurate parameters.* Calibrate the component lead temperature, time to reflow, and capability for component removal normal to the plane of the PCB to correlate to this set of recommendations.

SUMMARY

Intel recommends that three critical parameters be met to ensure electrical testability of a component* removed from printed circuit boards: (1) The solder must be completely molten before removal is initiated; (2) the removal direction must be normal to the plane of the board; and (3) no movement, in-plane or tilting, of the removed component should occur until the solder completely resolidifies. Intel recommends specific temperatures and dwell time at temperature as a function of package type and size.

NOTE:

*This pertains to components that have not been adhesively attached to the board for double-sided board usage.

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Shipping and Packing

7



CHAPTER 7 SHIPPING AND PACKING

PACKING MEDIA

Tubes

Plastic shipping and handling tubes are manufactured from polyvinyl chloride (PVC) with an antistatic surfactant treatment. Standard tubes for most package types are translucent and allow visual inspection of units within the tube. Carbon-impregnated, black conductive tubes are available for all parts, where required by device or use characteristics.

Tube profiles are designed with minimum clearance over the maximum package dimensions to reduce damaging movement of the device within the tube. For some package types, tubes have “riding rails” on which the packages rest while in the tube. The rails protect the fragile leads from touching anything in the tube. All tube wall thicknesses are 0.025 in. to 0.040 in. Tables 7-1 through 7-7 show tube dimensions, cross-sections, and quantity per tube for most Intel package types. Further information on new packages should be requested through Intel Field Sales.

Table 7-1. PLCC Shipping Tube Dimensions (In Inches)

Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
20L Square		0.030	19.375	0.480	0.263	45
28L Square		0.030	19.375	0.580	0.263	35
44L Square		0.025	19.375	0.780	0.250	25
52L Square		0.030	11.50	0.880	0.263	12
68L Square		0.025	11.50	1.090	0.250	9
28L Rectangular		0.025	19.375	0.480	0.220	30
32L Rectangular		0.025	19.375	0.580	0.220	30
84L Square		0.040	11.50	1.300	0.288	8

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Table 7-2. Cerquad Shipping Tube Dimensions (In Inches)

Lead Type	Cross Section (W x H)	Wall Thickness	Inside Dimensions			Quantity Per Tube
			Height (H)	Width (W)	Length (L)	
44SQ		0.030	0.200	0.730	11.50	11
52SQ		0.025	0.203	0.820	11.50	11
68SQ		0.030	0.200	1.040	11.50	9
28SQ		0.030	0.203	0.520	11.50	15
32R		0.030	0.175	0.530	11.50	12

Table 7-3. PQFP Shipping Tube Dimensions (In Inches)

Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
84L PQFP		0.030	9.50	0.999	0.280	10
100L PQFP		0.030	10.50	1.099	0.280	10
132L PQFP		0.030	12.50	1.299	0.280	10
164L PQFP		0.030	14.50	1.499	0.280	10
196L PQFP		0.030	16.50	1.699	0.280	10

Table 7-4. LCC Shipping Tube Dimensions (In Inches)

Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
18L		0.025	11.5	0.370	0.165	25
20L		0.025	11.5	0.370	0.165	25
28L		0.025	11.5	0.530	0.165	22
32L		0.025	11.5	0.535	0.207	18
44L		0.025	11.5	0.736	0.180	16
68L		0.025	11.5	1.060	0.235	10
32L J-Lead Rectangular		0.030	11.5	0.590	0.235	12
32L J-Lead Rectangular EPROM		0.030	11.5	0.600	0.260	16
44L J-Lead Square		0.025	11.5	0.786	0.250	15

Table 7-5. PGA Shipping Tube Dimensions (In Inches)

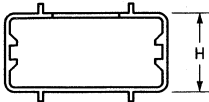
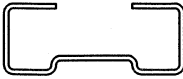
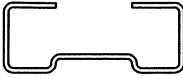
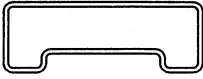


Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
68L		0.040	20	1.250	0.460	15
88L		0.050	20	1.470	0.720	12
132L		0.045	20	1.565	0.720	11

Table 7-6. Flatpack Shipping Tube Dimensions (In Inches)

Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
18L* Ceramic		0.020	20	0.810	0.290	18
68L Plastic		0.040	20	2.138	0.628	9
68L Ceramic Quadpack		0.035	20	2.120	0.610	9

*Aluminum Tube

Table 7-7. DIP Shipping Tube Dimensions (In Inches)

Lead Type	Cross Section (W x H)	Wall Thickness	Outside Dimensions			Quantity Per Tube
			Length (L)	Width (W)	Height (H)	
16L		0.020	20	0.600	0.510	24 (P) 23 (D) 23 (C)
18L		0.020	20	0.600	0.510	20 (P) 21 (D), (C)
20L		0.020	20	0.600	0.510	18 (P), (D) 17 (C)
24L (300 mil)		0.020	20	0.600	0.510	15
28L (300 mil)		0.020	20	0.600	0.510	14 (P) 13 (D)
22L (400 mil)		0.030	20	0.727	0.535	17
24L (600 mil)		0.022	20	0.890	0.495	15
28L (600 mil)		0.022	20	0.890	0.495	13
32L		0.022	20	0.890	0.495	11
40L		0.022	20	0.890	0.495	9
48L		0.022	20	0.890	0.495	7 (P) 8 (C)

NOTE:

- (P) = PDIP
- (C) = Ceramic Sidebraced
- (D) = CERDIP

CARRIERS

Additional protection from lead damage is necessary for the fragile leads of the flatpack packages, which are shipped flat to be trimmed and formed at the customer site. Plastic carriers are used to hold each unit, then the loaded carrier is placed in the tube. Carriers are coated with an antistatic surfactant treatment like the tubes, and may be manufactured from carbon-impregnated conductive PVC or nonconductive PVC, depending on the device. Figures 7-1 through 7-3 show a variety of carrier types.

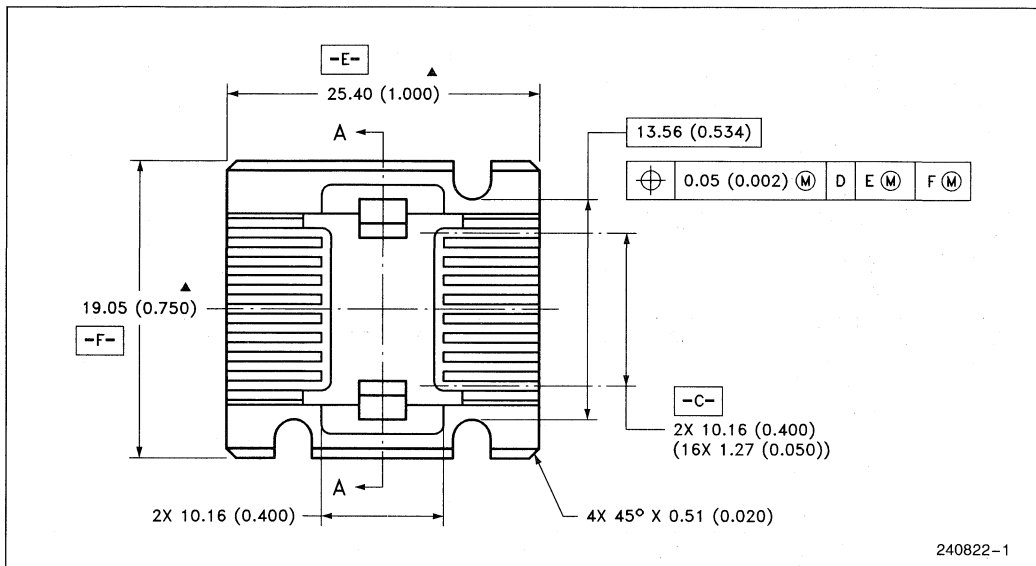


Figure 7-1. 18-Lead Ceramic Flatpack Carrier

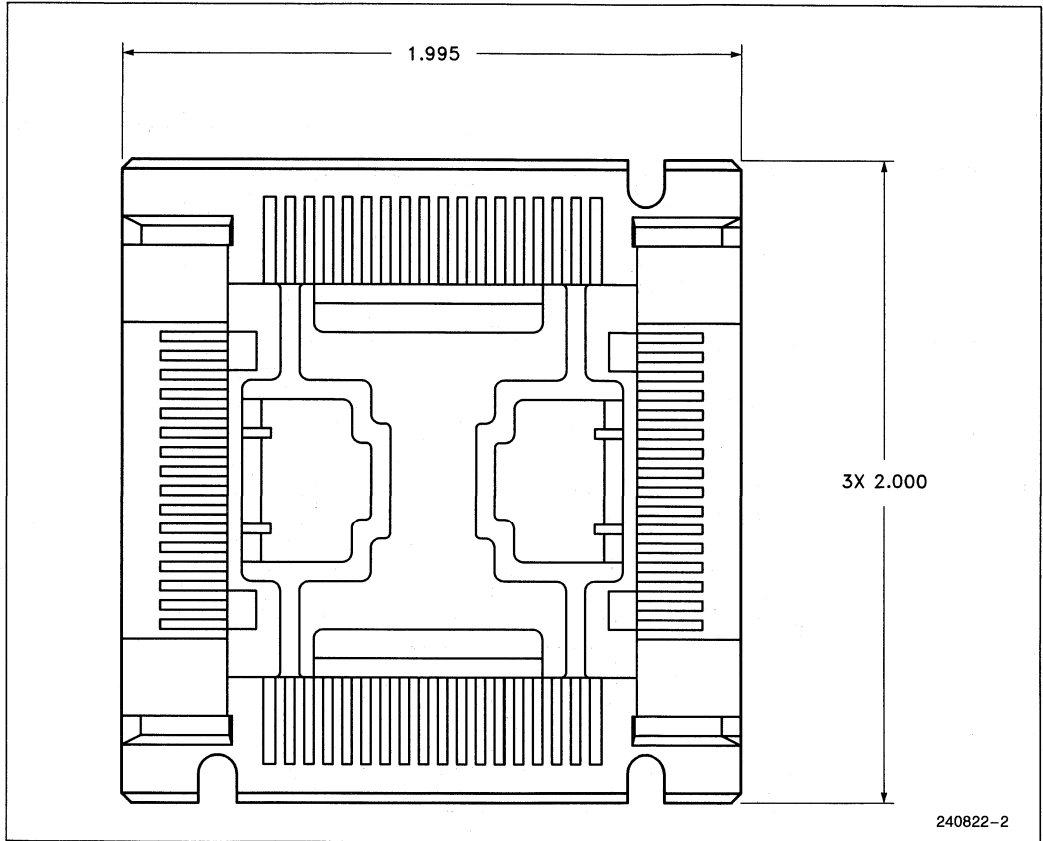


Figure 7-2. 68-Lead Ceramic Flatpack Carrier

Tape and Reel

The tape and reel packing system places PLCCs in a tape embossed with individual carrier pockets. The devices are then sealed with a cover tape to retain and protect them. The loaded tapes are next wound onto a reel similar to a movie reel. The number of devices per reel (or capacity per reel) will vary depending on the lead count of the devices involved. Tape and reel packing is growing in popularity, especially for PLCCs, because it preserves lead coplanarity.

The Electronics Industries Association (EIA) has set tape and reel standards for tapes measuring from 8mm to 56mm (EIA spec. RS-481-A), as shown in Figures 7-4 through 7-6 and Table 7-8. Standard reel size is 13 in.

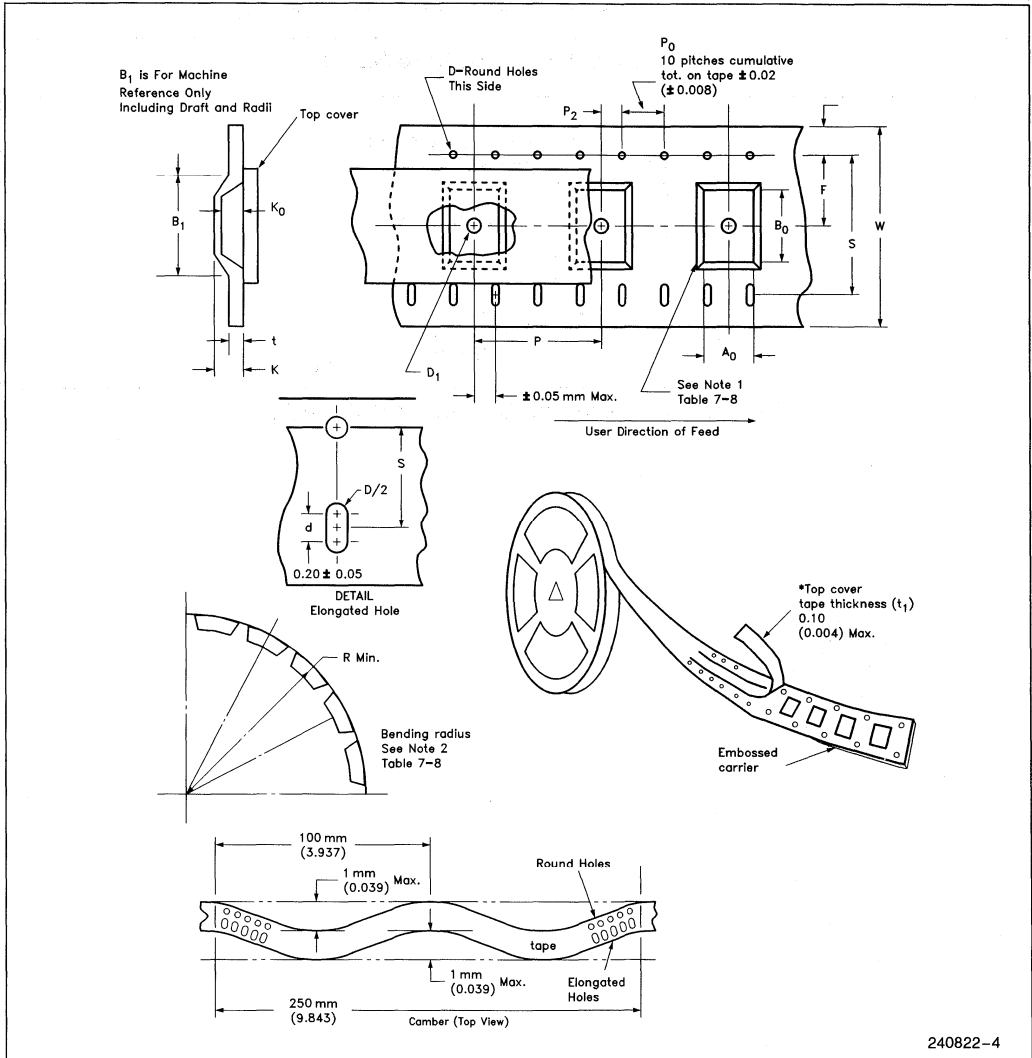


Figure 7-4. EIA, Tape and Reel Standard for IC Packages

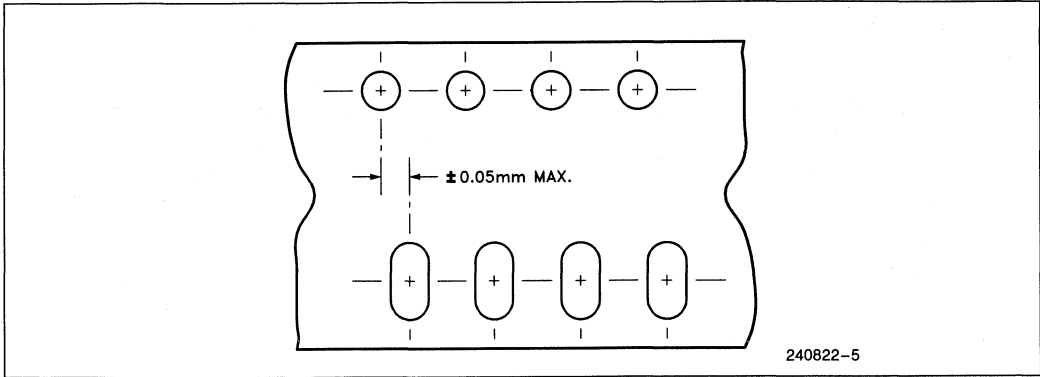


Figure 7-5. Sprocket Hole Skew

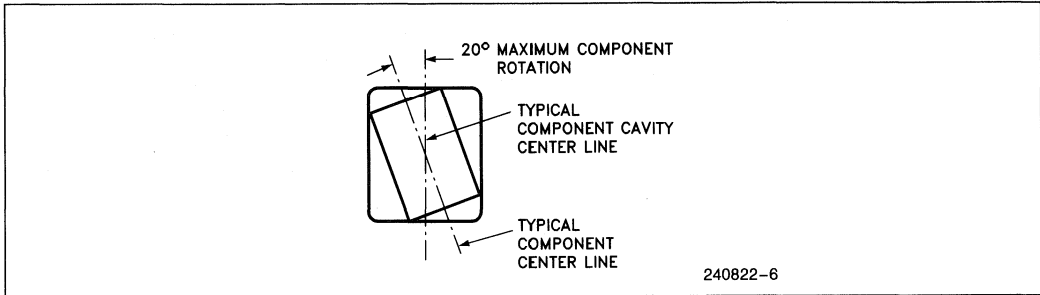


Figure 7-6. Maximum Component Rotation

Table 7-8. 32 mm, 44 mm, 46 mm, 46 mm Embossed Tape

Tape Size	D	D1 Min	E	K Max	P0	T Max	A0 B0 K0	Constant Dimensions
32 mm, 44 mm 56 mm	1.5 ^{+0.10} _{-0.0} [0.59 ^{+0.004} _{-0.0}]	2.0 [0.079]	1.75 ± 0.10 [0.089 ± 0.004]	10.0 [0.394]	4.0 ± 0.10 [0.156 ± 0.004]	0.500 [0.020]	See Note 1 Table 3	

Tape Size	B1 Max	F	P2	S	W	R Min	Variable Dimensions
32 mm	23.0 [0.906]	14.2 ± 0.10 [0.559 ± 0.004]	2.0 ± 0.10 [0.079 ± 0.004]	28.4 ± 0.10 [1.118 ± 0.004]	32.0 ± 0.30 [1.26 ± 0.12]	50.0 [1.973]	
44 mm	36.0 [1.375]	20.2 ± 0.15 [0.795 ± 0.006]	2.0 ± 0.15 [0.79 ± 0.006]	40.4 ± 0.10 [1.591 ± 0.004]	44.0 ± 0.30 [1.732 ± 0.12]	100.00 [3.94]	
58 mm	46.0 [1.811]	26.2 ± 0.15 [1.031 ± 0.006]		52.4 ± 0.10 [2.063 ± 0.004]	56.0 ± 0.30 [2.205 ± 0.12]		

Tape Size	P										
16 ± 0.10 [0.630 ± 0.004]	20.0 ± 0.10 [0.787 ± 0.004]	24 ± 0.10 [0.945 ± 0.004]	28.0 ± 0.10 [1.102 ± 0.004]	32.0 ± 0.10 [1.26 ± 0.004]	36.0 ± 0.10 [1.417 ± 0.004]	40 ± 0.10 [1.575 ± 0.004]	44.0 ± 0.10 [1.732 ± 0.004]	48.0 ± 0.10 [1.890 ± 0.004]	52.0 ± 0.10 [2.047 ± 0.004]	56.0 ± 0.10 [2.205 ± 0.004]	
32 mm	X	X	X	X							
44 mm		X	X	X	X	X	X	X			
56 mm						X	X	X	X	X	X

NOTES:

1. A₀, B₀, K₀ are determined by component size. The clearance between the component and the cavity must be within 0.05 [0.002] Min to 1.00 [0.039] Max. The component cannot rotate more than 20°C within the determined cavity, see Figure 4-15.
2. Tape and components shall pass around radius "R" without damage.

Trays

Intel offers trays for all PQFP and select PGA, LGA, cerquad, CQFP, and LCC package shipping, in addition to tubes. All TSOPs are shipped in trays. Shipping trays are JEDEC standard dimensions and can be baked to 125°C. The material of construction is high-temperature polyethersulfone (PES) chosen for its high deflection temperature, superior strength, and dimensional stability. All JEDEC trays have the same outside dimensions and are easily stacked for storage and manufacturing. The tray cavities are designed to prevent damage to the devices. QFP trays are EIAJ standard dimensions due to market demands, but are comparable in construction.

Detailed drawings of trays for PQFP, TSOP, and QFP packages are shown in Figures 7-7 through 7-9 and Tables 7-9 through 7-10. Several other package types are available in trays by special order; Intel field sales engineers can obtain drawings and specifications upon request.

Table 7-9a. PQFP Tray for Handling and Shipping

Symbol	Variations (All Dimensions Are in Inches)											
	AA		Note	AB		Note	AC		Note	AD		Note
	Min	Max		Min	Max		Min	Max		Min	Max	
J	0.594	0.599		0.694	0.699		0.794	0.799		0.894	0.899	
J1	0.385	0.395		0.485	0.495		0.585	0.595		0.685	0.695	
J2	0.395	0.405		0.495	0.505		0.595	0.605		0.695	0.705	
J3	0.265	0.275		0.365	0.375		0.465	0.475		0.565	0.575	
J4	(0.277)		4	(0.322)		4	(0.276)		4	(0.270)		4
J5	(0.409)		4	(0.424)		4	(0.409)		4	(0.400)		4
J6	(0.205)		4	(0.220)		4	(0.205)		4	(0.196)		4
J7	(0.175)		4	(0.220)		4	(0.174)		4	(0.168)		4
K	0.594	0.599		0.694	0.699		0.794	0.799		0.894	0.899	
K1	0.385	0.395		0.485	0.495		0.585	0.595		0.685	0.695	
K2	0.395	0.405		0.495	0.505		0.595	0.605		0.695	0.705	
K3	0.265	0.275		0.365	0.375		0.465	0.475		0.565	0.575	
K4	(0.230)		4	(0.238)		4	(0.271)		4	(0.221)		4
K5	(0.315)		4	(0.333)		4	(0.397)		4	(0.297)		4
K6	(0.111)		4	(0.129)		4	(0.193)		4	(0.093)		4
K7	(0.128)		4	(0.136)		4	(0.169)		4	(0.119)		4
M	0.560			0.618			0.701			0.701		
M1	0.607			0.717			0.706			0.750		
M2	0.799			0.914			0.999			1.090		
M3	0.705			0.823			0.987			0.987		
N	52		7	68		7	84		7	100		7
N1	7		8	6		8	5		8	5		8
N2	15		8	13		8	12		8	11		8
N3	105		8	78		8	60		8	55		8
R	0.120	0.130		0.120	0.130		0.185	0.195		0.185	0.195	
R1	0.057	0.067		0.057	0.067		0.120	0.130		0.120	0.130	
Y1	3.945	3.955	2	4.445	4.455	2	4.945	4.955	2	5.445	5.455	2
Note	1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10		



PACKAGING

Table 7-9b. PQFP Tray for Handling and Shipping

Symbol	Variations (All Dimensions Are in Inches)											
	AA		Note	AB		Note	AC		Note	AD		Note
	Min	Max		Min	Max		Min	Max		Min	Max	
J	15.09	15.21		17.63	17.75		20.17	20.29		22.71	22.83	
J1	9.78	10.03		12.32	12.57		14.86	15.11		17.40	17.65	
J2	10.03	10.29		12.57	12.83		15.11	15.37		17.65	17.91	
J3	6.73	6.98		9.27	9.52		11.81	12.07		14.35	14.60	
J4	(7.04)		4	(8.18)		4	(7.01)		4	(6.86)		4
J5	(10.39)		4	(10.77)		4	(10.39)		4	(10.16)		4
J6	(5.21)		4	(5.59)		4	(5.21)		4	(4.98)		4
J7	(4.45)		4	(5.59)		4	(4.42)		4	(4.27)		4
K	15.08	15.21		17.62	17.75		20.16	20.29		22.70	22.83	
K1	9.78	10.03		12.32	12.57		14.86	15.11		17.40	17.65	
K2	10.03	10.29		12.57	12.83		15.11	15.37		17.65	17.91	
K3	6.73	6.98		9.27	9.52		11.81	12.07		14.35	14.60	
K4	(5.84)		4	(6.05)		4	(6.88)		4	(5.61)		4
K5	(8.00)		4	(8.46)		4	(10.09)		4	(7.55)		4
K6	(2.82)		4	(3.28)		4	(4.91)		4	(2.37)		4
K7	(3.25)		4	(3.46)		4	(4.29)		4	(3.02)		4
M	14.22			15.70			17.81			17.81		
M1	15.42			18.21			17.93			19.05		
M2	20.29			23.21			25.37			27.69		
M3	17.91			20.90			25.07			25.07		
N	52		7	68		7	84		7	100		7
N1	7		8	6		8	5		8	5		8
N2	15		8	13		8	12		8	11		8
N3	105		8	78		8	60		8	55		8
R	3.05	3.30		3.05	3.30		4.70	4.95		4.70	4.95	
R1	1.45	1.70		1.45	1.70		3.05	3.30		3.05	3.30	
Y1	100.20	100.46	2	112.90	113.16	2	125.60	125.86	2	138.30	138.56	2
Note	1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10		

Table 7-9c. PQFP Tray for Handling and Shipping

Symbol	Variations (All Dimensions Are in Inches)											
	AA		Note	AB		Note	AC		Note	AD		Note
	Min	Max		Min	Max		Min	Max		Min	Max	
J	1.094	1.099		1.294	1.299		1.494	1.499		1.794	1.799	
J1	0.885	0.895		1.085	1.095		1.285	1.295		1.585	1.595	
J2	0.895	0.905		1.095	1.105		1.295	1.305		1.595	1.605	
J3	0.765	0.775		0.965	0.975		1.165	1.175		1.465	1.475	
J4	(0.322)		4	(0.277)		4	(0.284)		4	(0.275)		4
J5	(0.424)		4	(0.408)		4	(0.422)		4	(0.408)		4
J6	(0.220)		4	(0.204)		4	(0.218)		4	(0.204)		4
J7	(0.220)		4	(0.175)		4	(0.182)		4	(0.173)		4
K	1.094	1.099		1.294	1.299		1.494	1.499		1.794	1.799	
K1	0.885	0.895		1.085	1.095		1.285	1.295		1.585	1.595	
K2	0.895	0.905		1.095	1.105		1.295	1.305		1.595	1.605	
K3	0.765	0.775		0.965	0.975		1.165	1.175		1.465	1.475	
K4	(0.244)		4	(0.322)		4	(0.250)		4	(0.322)		4
K5	(0.344)		4	(0.424)		4	(0.355)		4	(0.424)		4
K6	(0.140)		4	(0.220)		4	(0.151)		4	(0.220)		4
K7	(0.142)		4	(0.220)		4	(0.148)		4	(0.220)		4
M	0.824			1.161			1.030			1.668		
M1	0.944			0.957			1.064			1.205		
M2	1.314			1.498			1.712			1.998		
M3	1.234			1.514			1.645			2.014		
N	132		7	164		7	196		7	244		7
N1	4		8	3		8	3		8	2		8
N2	9		8	8		8	7		8	6		8
N3	36		8	24		8	21		8	12		8
R	0.185	0.195		0.185	0.195		0.185	0.195		0.185	0.195	
R1	0.120	0.130		0.120	0.130		0.120	0.130		0.120	0.130	
Y1	5.945	5.955	2	6.445	6.455	2	6.945	6.955	2	7.445	7.455	2
Note	1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10		

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Table 7-9d. PQFP Tray for Handling and Shipping

Symbol	Variations (All Dimensions Are in Inches)											
	AA		Note	AB		Note	AC		Note	AD		Note
	Min	Max		Min	Max		Min	Max		Min	Max	
J	27.79	27.91		32.87	32.99		37.95	38.07		45.57	45.69	
J1	22.48	22.73		27.56	27.81		32.64	32.89		40.26	40.51	
J2	22.73	22.99		27.81	28.07		32.89	33.15		40.51	40.77	
J3	19.43	19.68		24.51	24.76		29.59	29.84		37.21	37.46	
J4	(8.18)		4	(7.04)		4	(7.21)		4	(6.99)		4
J5	(10.77)		4	(10.36)		4	(10.72)		4	(10.36)		4
J6	(5.59)		4	(5.18)		4	(5.54)		4	(5.18)		4
J7	(5.59)		4	(4.44)		4	(4.62)		4	(4.39)		4
K	27.78	27.91		32.86	32.99		37.94	38.07		45.56	45.69	
K1	22.48	22.73		27.56	27.81		32.64	32.89		40.26	40.51	
K2	22.73	22.99		27.81	28.07		32.89	33.15		40.51	40.77	
K3	19.43	19.68		24.51	24.76		29.59	29.84		37.21	37.46	
K4	(6.20)		4	(8.18)		4	(6.35)		4	(8.18)		4
K5	(8.74)		4	(10.77)		4	(9.02)		4	(10.77)		4
K6	(3.56)		4	(5.59)		4	(3.84)		4	(5.59)		4
K7	(3.61)		4	(5.59)		4	(3.76)		4	(5.59)		4
M	20.93			29.49			29.16			42.37		
M1	23.98			24.31			27.03			30.61		
M2	33.37			38.05			43.48			50.75		
M3	31.34			38.46			41.78			51.16		
N	132		7	164		7	196		7	244		7
N1	4		8	3		8	3		8	2		8
N2	9		8	8		8	7		8	6		8
N3	36		8	24		8	21		8	12		8
R	4.70	4.95		4.70	4.95		4.70	4.95		4.70	4.95	
R1	3.05	3.30		3.05	3.30		3.05	3.30		3.05	3.30	
Y1	151.00	151.26	2	163.70	163.96	2	176.40	176.66	2	189.10	189.36	2
Note	1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10			1, 5, 5a, 6, 9, 10		

Table 7-9e

NOTES:

- △ These surfaces to be free of mold seams.
- △ The fifth notch assists in the visual or mechanical orientation of the tray. Its position along the left side of the tray indicates the specific package family, allowing the visual determination that all trays within a stack are of the same type.
- △ Chamfer denotes package pin 1 orientation.
- △ Reference dimensions K₄ through K and J₄ through J are associated with tray partitions. In some cases, partitions along the tray perimeter will not be in contact with the inside surface of the edge of the tray. Any "free" side of any partition shall have a 7° draft angle.

VACUUM PICKUP OF EMPTY TRAYS:

- △ Method one requires two separate pickup areas, resulting in two solid pedestals per tray. Locations of solid pedestals (see Detail D) are listed here by [Row #, Column #], 2 locations for each tray:

AA [4,4] [12,4]	AE [2,2] [8,3]
AB [3,3] [11,4]	AF [2,2] [7,2]
AC [3,3] [10,3]	AG [2,2] [6,2]
AD [3,3] [7,3]	AH [2,1] [5,2]
- △ Method two requires one "fenced pocket" with solid pedestal located near the center of each tray. The locations, also listed by [Row #, Column #] are as follows:

AA [8,4]	AE [5,2]
AB [7,3]	AF [4,2]
AC [6,3]	AG [4,2]
AD [6,3]	AH [3,1]
- △ This groove allows the use of a pin to mechanically bias the tray orientation.
- △ The symbol N refers to the PQFP Package lead count supported.
- △ $N_3 = N_1 \times N_2$ (Total Tray Cavities).
- △ Non-tabulated dimensions are assumed to have a tolerance of $\pm \div 0.12$ (0.005).
- △ Interpret dimensions and tolerances in accordance with ANSI Y14.5M-1982.

Table 7-10. QFP Tray for Handling and Shipping (Typical)

Lead Count	Quantity per Tray	Trays per Box
44	50	10
48	40	10
64	64	10
80	64	10
208	—	—

NOTE:

Not all products are available in all packages. Contact your local Intel FSE for the specific availability.

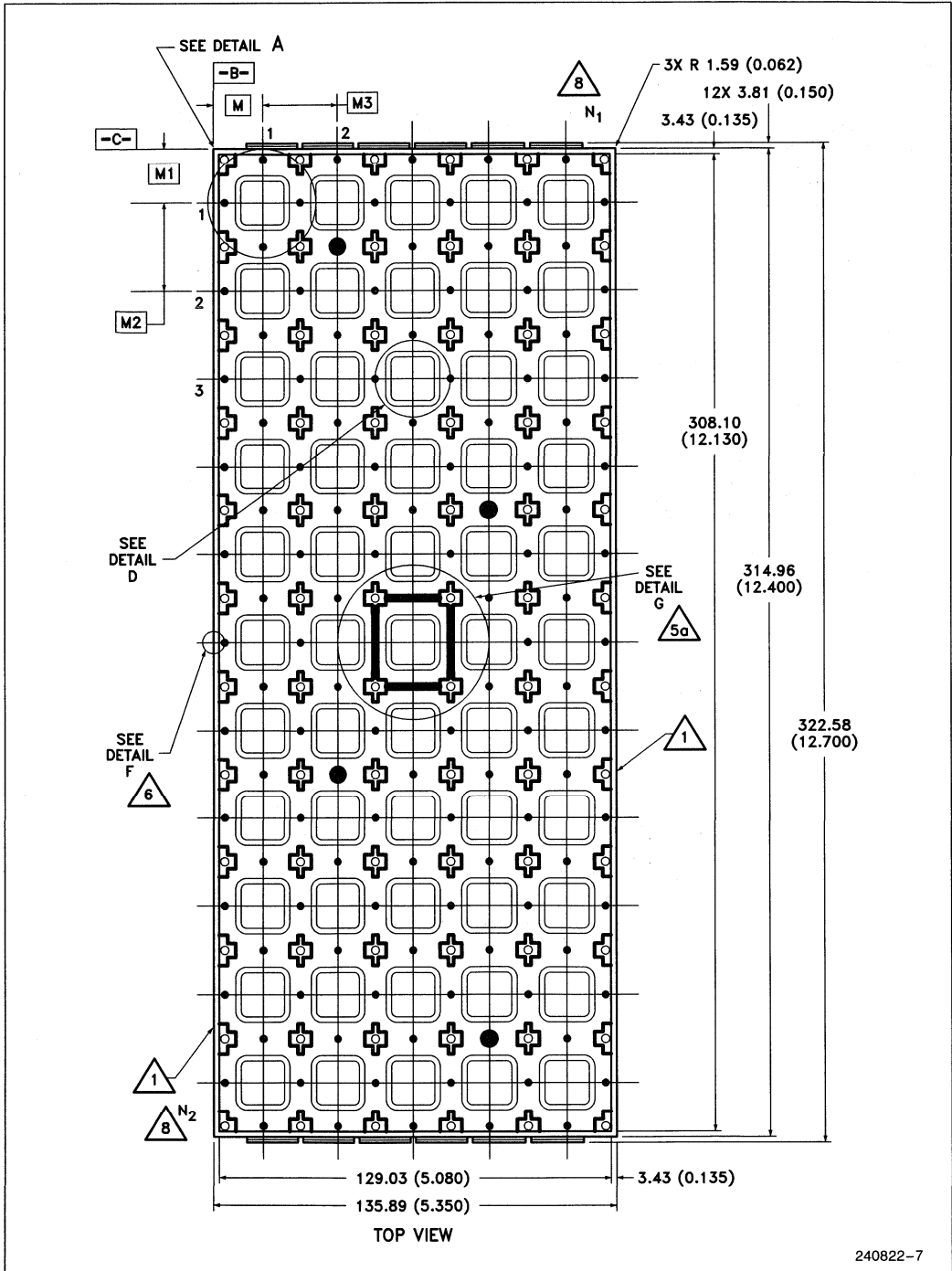


Figure 7-7a. PQFP Tray for Handling and Shipping

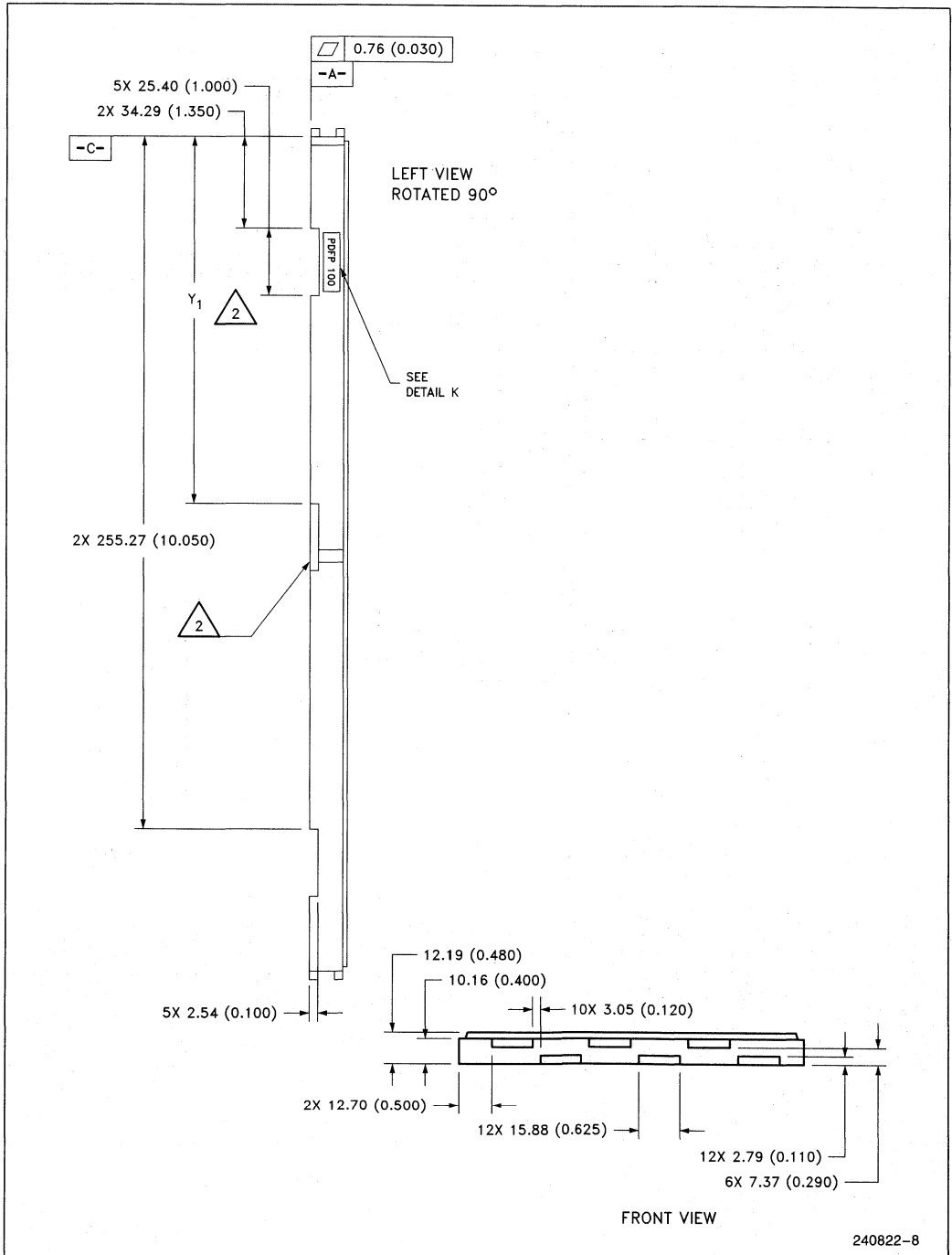


Figure 7-7b. PQFP Tray for Handling and Shipping

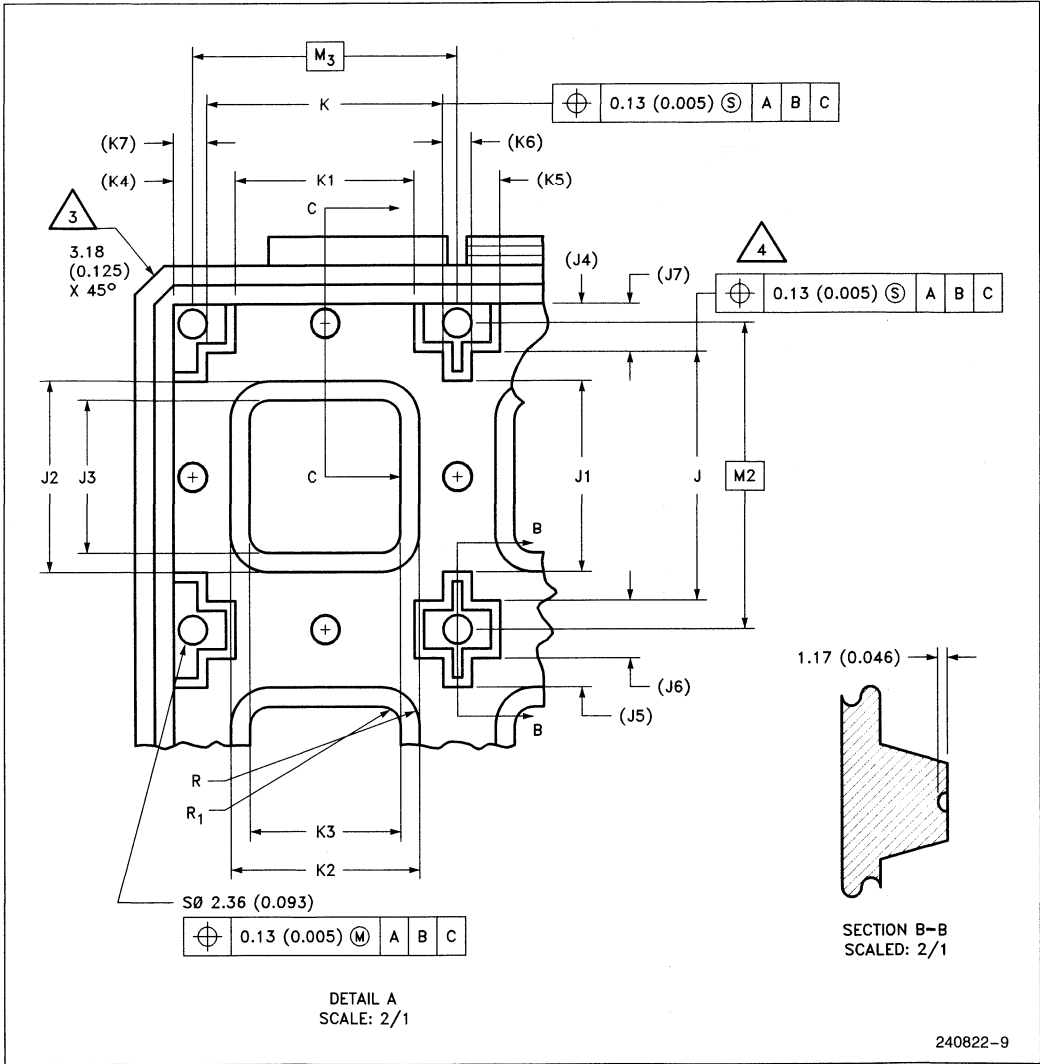


Figure 7-7c. PQFP Tray for Handling and Shipping

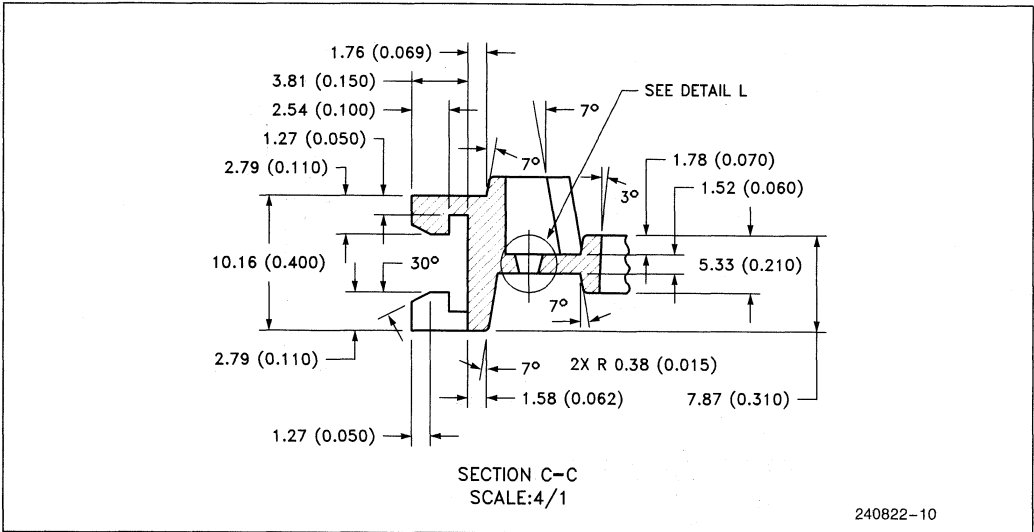


Figure 7-7d. PQFP Tray for Handling and Shipping

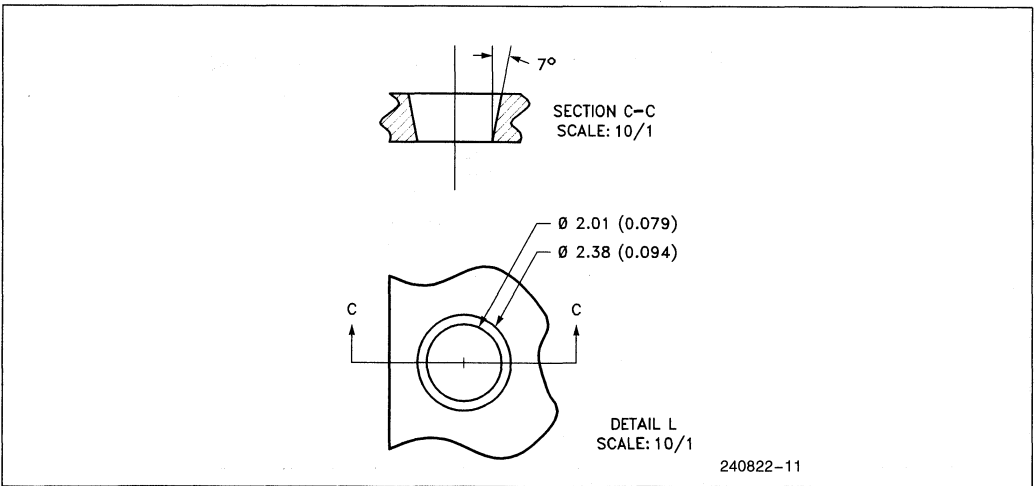


Figure 7-7e. PQFP Tray for Handling and Shipping

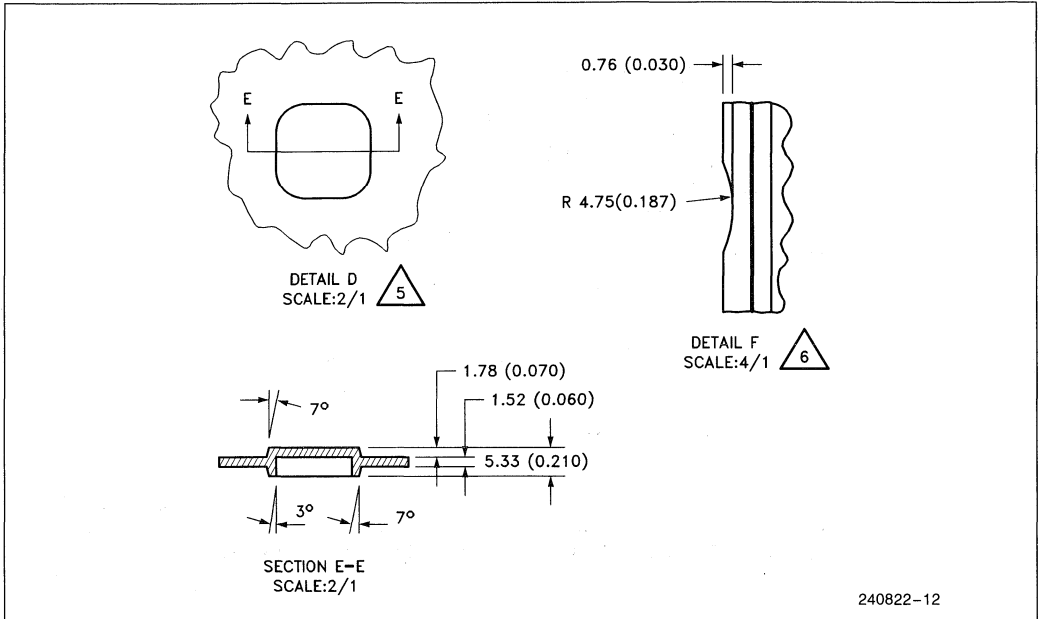


Figure 7-7f. PQFP Tray for Handling and Shipping

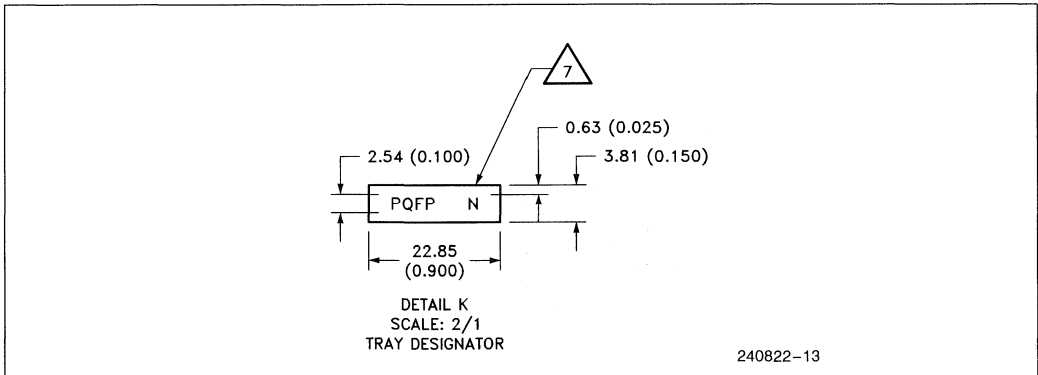


Figure 7-7g. PQFP Tray for Handling and Shipping

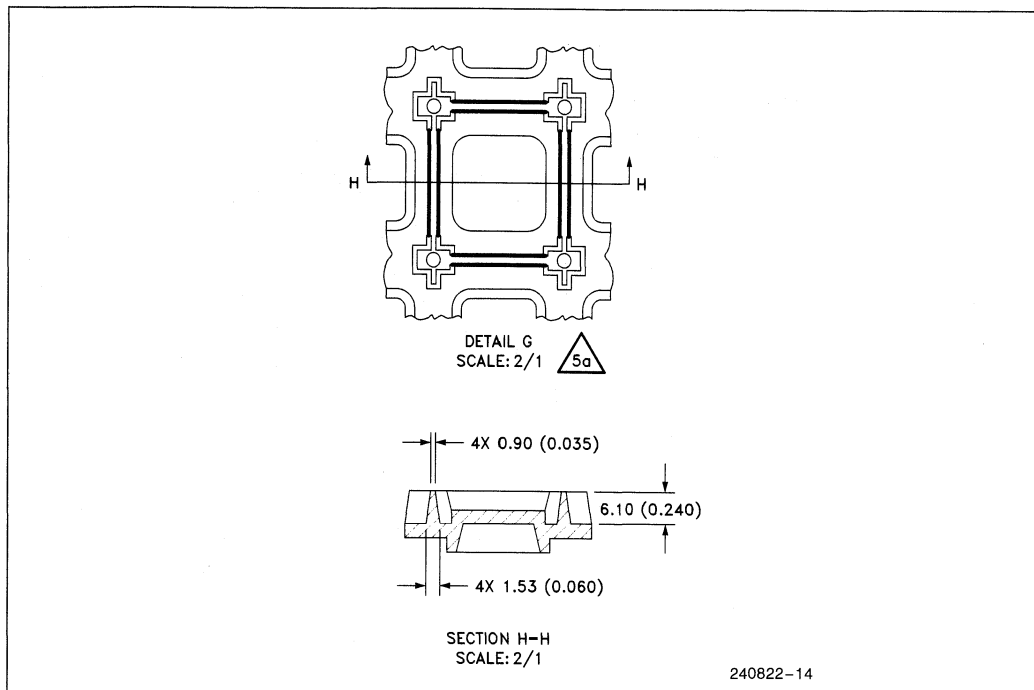
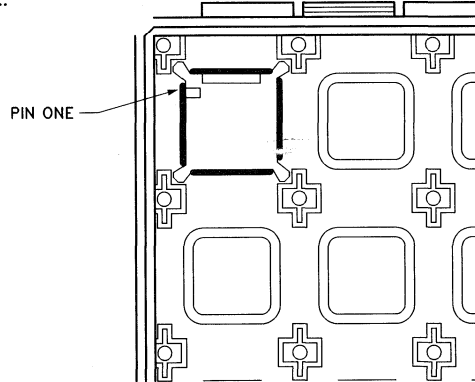


Figure 7-7h. PQFP Tray for Handling and Shipping

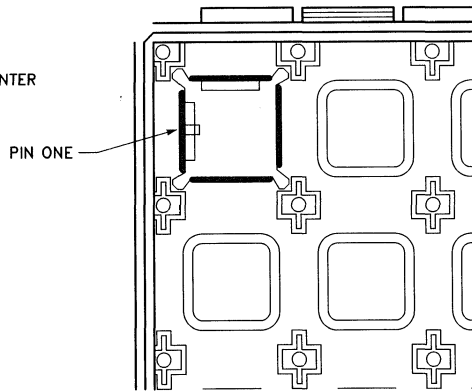
APPLICATIONS

PACKAGE ORIENTATION IN THE TRAY:

FOR PACKAGES WITH PIN 1
IN THE CORNER...

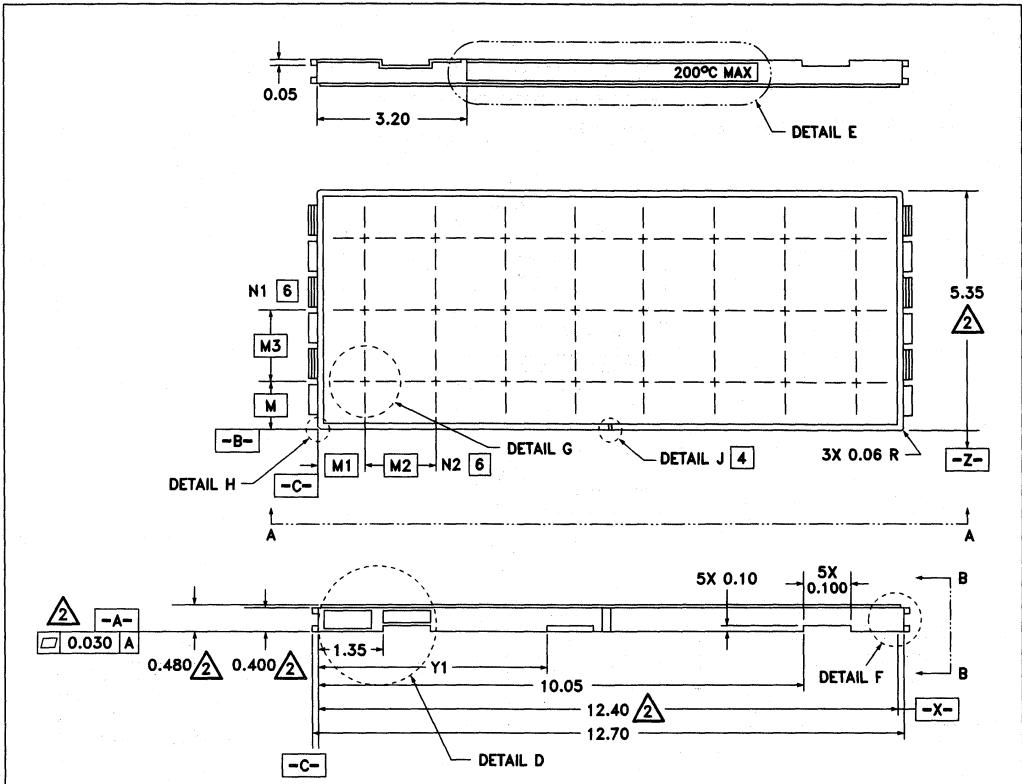


..AND IN THE CENTER



240822-15

Figure 7-7i. PQFP Tray for Handling and Shipping



240822-16

NOTES:

- 1 Material: PES (polyethersulfone) statically dissipative carbon-filled.
- 2 Critical inspection dimension.
- 3 Chamfer denotes package pin one orientation.
- 4 The notch allows the use of a pin to mechanically bias the tray orientation.
- 5 The symbol N refers to the package lead count supported.
- 6 The symbol N1 refers to the number of rows. The symbol N2 refers to the number of columns. The symbol N3 refers to the total number of pockets ($N1 \times N2$) for the lead count supported.
- 7 All dimensions are reported in millimeters.

Figure 7-8a. Tray Dimensional Drawings

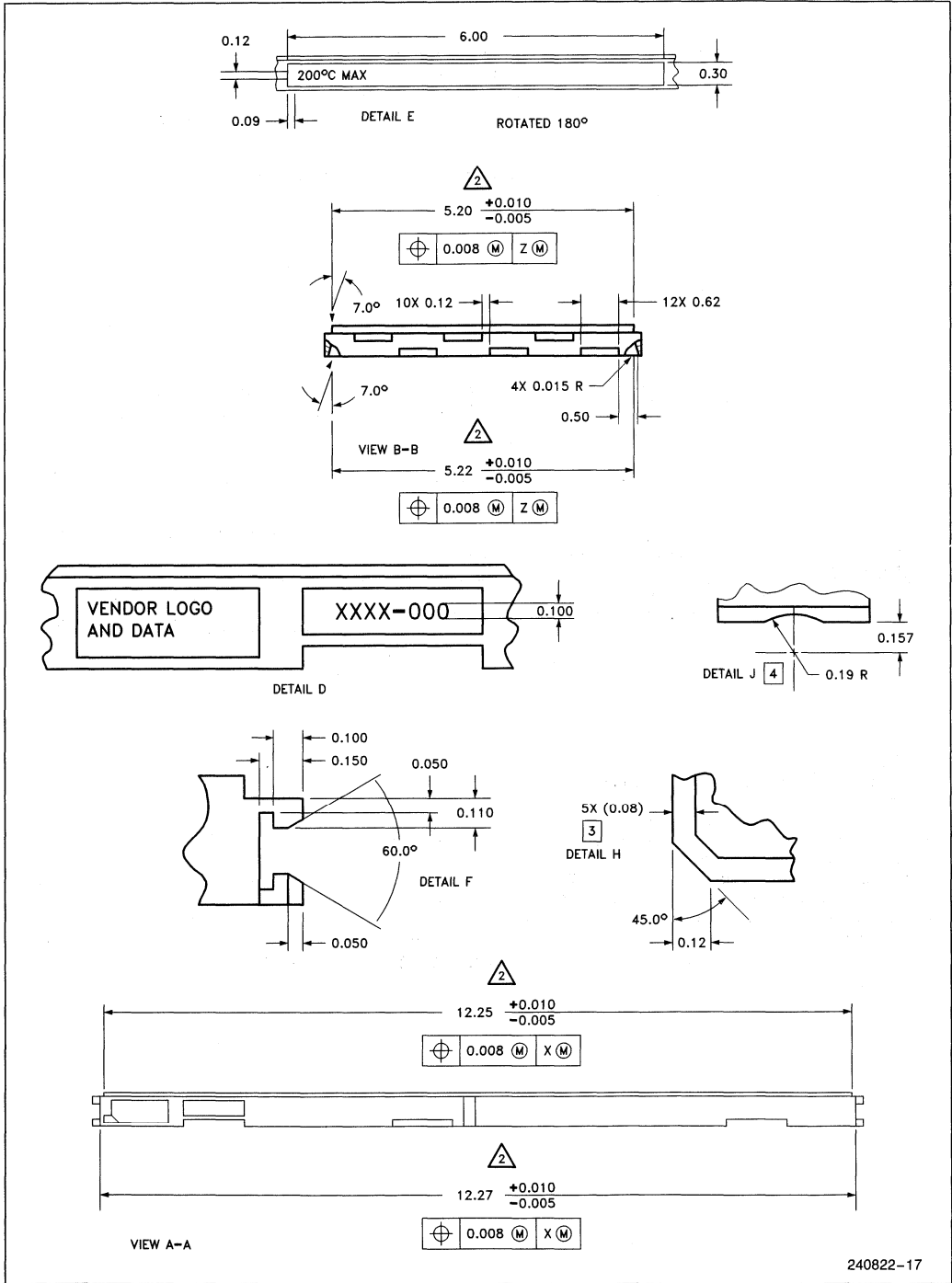


Figure 7-8b. Tray Dimensional Drawings

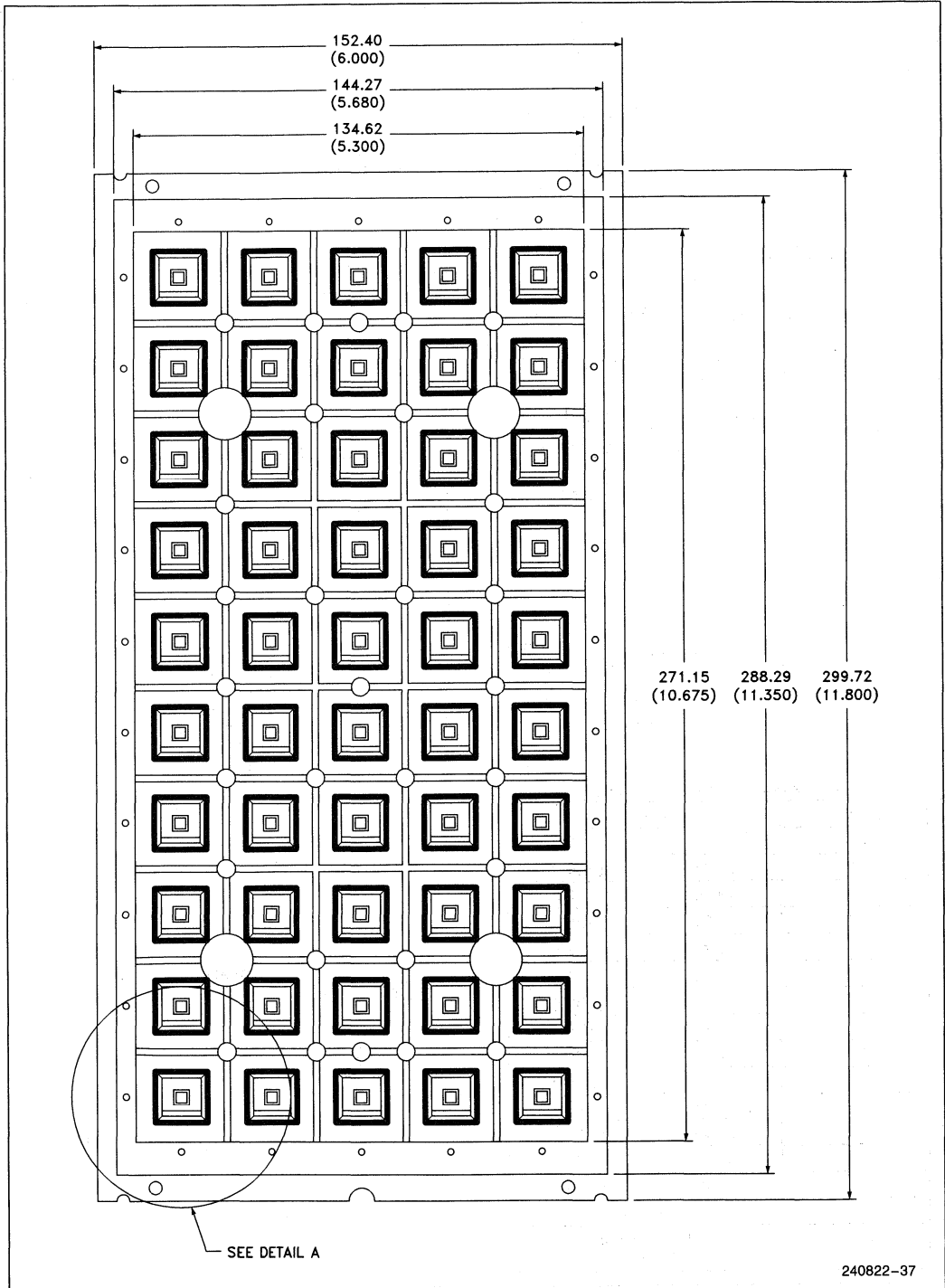


Figure 7-9a. QFP Tray for Handling and Shipping

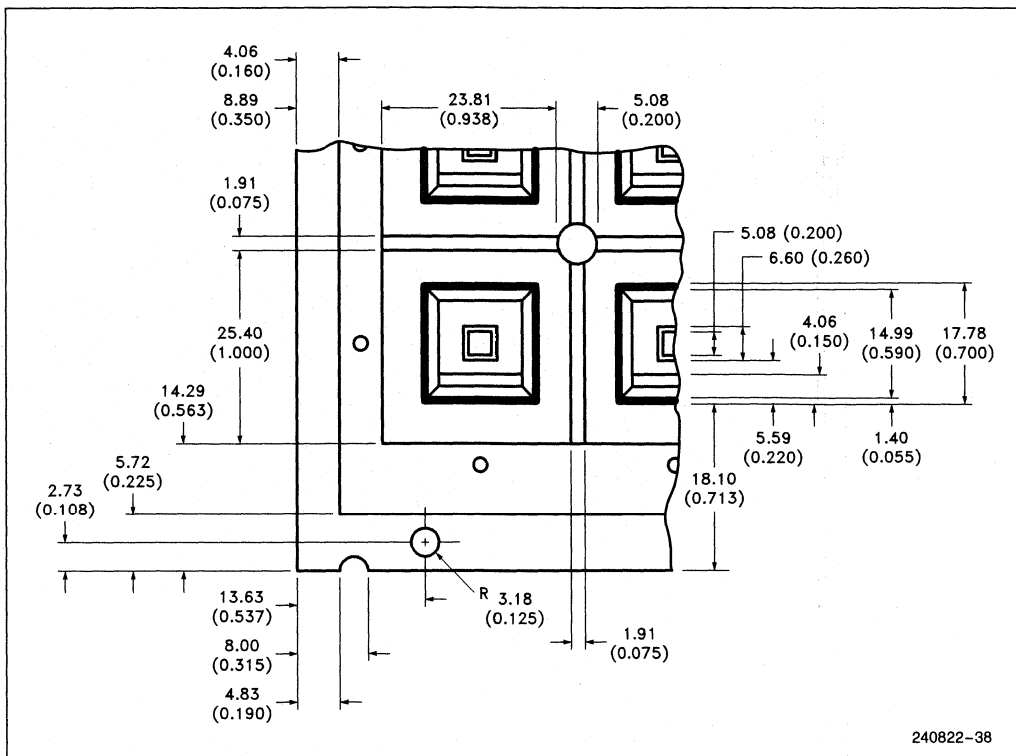


Figure 7-9b. Close-Up View of QFP Tray for Handling and Shipping

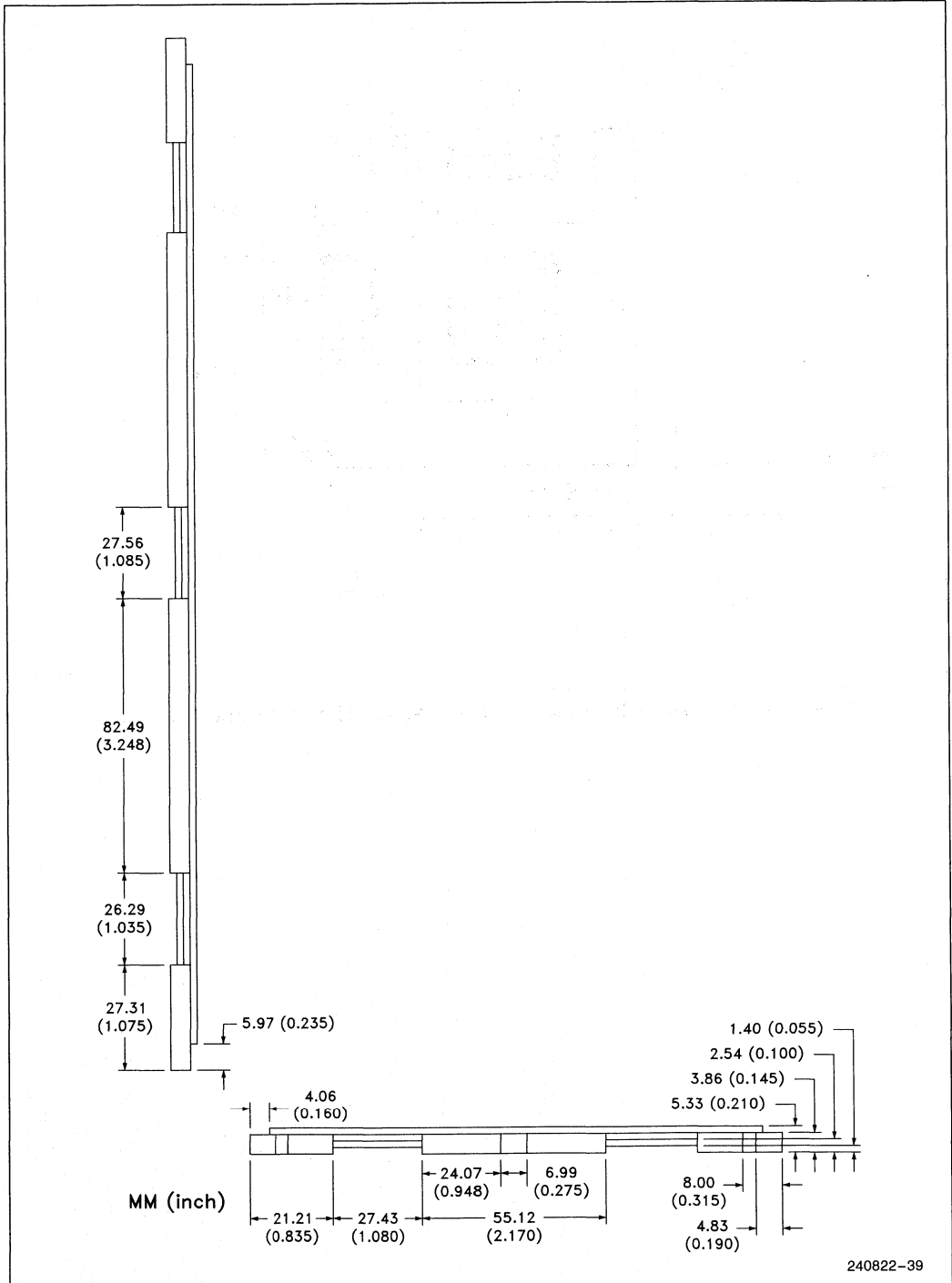


Figure 7-9c. QFP Tray for Handling and Shipping

SHIPPING FORMATS

Desiccant Pack Materials

All PSMCs are shipped in desiccant pack. For a thorough discussion of the packing process (bake and bag) and handling considerations unique to PSMCs, please consult Chapter 6, which addresses surface mount technology.

Intel uses the following materials in desiccant pack:

- **Moisture Barrier Bag (MBB).** Inside the shipping box is a moisture barrier bag containing components. The opaque MBB is constructed of three layers: a conductive polyethylene inner layer for sealing, an aluminum film mid-layer, and an aluminized tyvek outer layer. The bag meets MIL-STD-81705B TYPE I for electrostatic discharge (ESD) and mechanical stability. The measured water vapor transmission rate (WVTR) of the bag is better than the MIL-STD requirements for moisture protection. The $WVTR = 0.004 \text{ gr}/100 \text{ sq. in.}/24 \text{ hrs.}$ as measured at $40^\circ\text{C}/85\% \text{ RH}$.

A “warning” label on the bag outlines precautions that should be taken with desiccant-packed units. A desiccant barcode label is also affixed to the bag.

- **Desiccant.** Each MBB contains one or more pouches of silica gel desiccant to absorb moisture that may be present in the bag. The silica gel desiccant is supplied in two-unit (50-gram) pouches. The number of pouches required is a function of the bag surface area. The saturation limit for silica gel at 10% RH is 6.8% by weight at 25°C .
- **Humidity Indicator Card (HIC).** Along with the desiccant pouches, each MBB contains a humidity indicator card. This card is a military-standard moisture indicator and is included to show the user the approximate relative humidity (RH) level within the bag. The HIC is reversible and can be reused. A representation of the HIC is shown in Figure 7-19.
- **Labels.** The desiccant barcode label (shown in Figure 7-10), mentioned above in the section on MBBs, contains the date that the bag was sealed (MM/DD/YY). The remaining storage life of the units in the bag is determined from this date.

The “warning” label (see Figure 6-18) attached to the outside of the MBB outlines precautions that must be taken when handling desiccant-packed units if they are to be kept dry.

- **Shipping Box.** The shipping box will be the same in appearance as Intel’s standard shipping box, but the barcode label will indicate that desiccant-packed material is included. This label will indicate the seal date of the enclosed MBB, and thus, the remaining shelf life.

Shipping Boxes and Cartons

Intel products are placed in tubes or trays, or on reels, then packed for shipment in a box made of corrugated fiberboard with an inner coating of carbon to provide a Faraday shield that prevents electrostatic damage. Various materials, such as bubble wrap or antistatic foam end pads, are used for cushioning inside the box. Outer boxes are used for increased protection during shipping. All packing materials are either conductive, static dissipative, or antistatic, and meet the electrostatic discharge (ESD) requirements of EIA standard 541.

Tables 7-11 through 7-12b show box dimensions, the quantity of tubes per box, and the quantity of trays per box.

Table 7-11. Box Dimensions (In Inches)

Use	Inside Dimensions		
	Length (L)	Width (W)	Height (H)
20" Tubes 19.375" Tubes	21	5.75	2.75
11.5" Tubes JEDEC Trays	14	7	4
Reels	15	15	3

Table 7-12a. Quantity of Tubes per Box

Package Type	Lead Count	Tubes/Box
PLCC	18	84
	20SQ/28R	56
	28SQ/32R	42
	44SQ	28
	52SQ	60
	68SQ	48
	84SQ	36
Cerquad	28SQ/32R	90
	44SQ/52SQ	70
	68SQ	60
PQFP	84	16
	100	12
	132	10
	164	8
	196	6
LCC	18	200
	20/28/32	160
	68	60
PGA	44/68	12
	88/132	9
Flatpack	18	30
	68	8
DIP	300 mil	36
	400 mil	32
	600 mil	20
ZIP	20	88
SOJ	26	84

International Packaging Specifications

8



CHAPTER 8 INTERNATIONAL PACKAGING SPECIFICATIONS

ELECTRONIC INDUSTRIES ASSOCIATION OF JAPAN (EIAJ)

EIAJ publishes the following general rules and standards as they apply to preparation of outline drawings on integrated circuits:

Number	Nomenclature
SD-74-1	General rules for the preparation of outline drawings of semiconductor devices
SD-74-2	Outline drawings of semiconductor devices
SD-74-2 add 1	Outline drawings of semiconductor devices -1
SD-74-2 add 2	Outline drawings of semiconductor devices -2
IC-74-1	Outline drawings of integrated circuits
ED-7402	Small outline packages (SOPs)
IC-74-2	Thin small outline packages (TSOPs)
ED-7403-1	Dual in-line packages (DIPs)
IC-74-4	Quad flat packages (QFPs)
ED-7404-1	Quad flat packages (QFPs, fine pitch)
IC-74-5	Zig-zag in-line packages (ZIPs)
ED-7406	Small outline J-lead packages (SOJs)
ED-7407	Quad flat J-lead packages (QFPs)
ED-7408	Pin grid array packages (PGAs)
ED-7413	Small in-line packages (SIPs)

JOINT ELECTRON DEVICE ENGINEERING COUNCIL (JEDEC)

JEDEC Publication 95 lists all package outlines.

MIL STANDARDS

The following military standards include specifications required to meet U.S. Military requirements:

- MIL-M-38510 General Specifications for Microcircuits
- MIL-STD-883 Test Methods/Procedures for Microelectronics

**SEMICONDUCTOR EQUIPMENT AND MATERIALS INSTITUTE, INC.
(SEMI) STANDARDS**

For a list of SEMI standards, reference the *Book of SEMI Standards*, 1990, Vol. 4, Packaging Division, 605 E. Middlefield Road, Mountain View, CA 94043, U.S.A. Phone: (415) 964-5111. FAX: (415) 967-5375. TELEX: 856-777 SEMI-MNTV.

**INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS
(IPC) STANDARDS**

Number	Nomenclature
ANSI/IPC-S-815B	General requirements for soldering electronic connections
ANSI/IPC-SM-780	Component packaging and inter-connecting, with emphasis on surface mounting
ANSI/IPC-SM-782	Surface mount land patterns
IPC-SM-786	Impact of moisture on plastic I/C package cracking

For a list of additional IPC standards, contact: IPC, 7380 N. Lincoln Ave., Lincolnwood, Illinois, 60646. Phone: (708) 677-2850.



CHAPTER 9 GLOSSARY

A

Access hole: A hole or series of holes in successive layers of a multilayer board that provide(s) access to the surface of the land in one or more layers of the board.

Advanced Manufacturing Module (AMM): An engineering development line at Intel where processes/products are engineered and fully characterized before introduction to assembly production lines.

All-metal package: A hybrid circuit package made solely of metal, excluding glass or ceramic.

Alternating current resistance: The resistance offered by any circuit to the flow of alternating current.

Alumina: Aluminum oxide. Alumina substrates are made of formulations that are primarily alumina.

Ambient: The environment that surrounds a system or component.

Ampere: The unit used for measuring the quantity of an electric current flow. One ampere represents a flow of one coulomb per second.

Annular ring: The portion of a conductive material that completely surrounds a hole.

Anode: The electrode from which the forward current flows within a device.

Application-specific integrated circuit (ASIC): An integrated circuit chip customized for a specific product.

Area array tape-automated bonding: Tape-automated bonding in which edge-located pads and additional pads on the inner surface area of a chip are addressed in the bonding scheme.

ATME: Assembly/Test Manufacturing Engineering.

A/T QRE: Assembly/Test Quality & Reliability Engineering.

Auger: A surface analysis technique for detecting the chemical composition of material.

B

Base plane: The plane through the lowest point of the mounting surface of the package, except for packages using stand-offs.

Bipolar: A device in which both majority and minority carriers are present. Bipolar and metal-oxide semiconductor (MOS) are the two most common device types.

Body: The main or largest portion of a connector, to which other portions are attached or connected.

Bonding: The joining of two materials; for example, the attachment of wires to an integrated circuit or the mounting of an integrated circuit to a substrate.

Bonding pads: Areas of metallization on the integrated circuit die that permit connection of fine wires or circuit elements to the die.

Bond schedule: Bonding machine set-up parameters.

Bond window: The acceptable range of each bonding variable, including time, force, power, and temperature.

Bump: A means of providing a connection to the terminal area of a device. A small mound is formed on the device or substrate pads and is used as a contact for facedown bonding.

Bump contacts: Contacting pads that rise substantially above the surface level of the chip.

Bumped tape: A tape used in the tape-automated bonding process whose innerlead bond sites have been formed into raised metal bumps, thus eliminating the need for bumps on the chip itself.

Buried via: A via hole not extending to the surface.

Burn-in: The process of screening out marginal component parts by exposing them to elevated temperatures and voltage stress.

Butt lead: A lead count of surface mount devices in which pin tips contact the PC board.

C

Ceramic: Inorganic, nonmetallic, clay, or glasslike material whose final characteristics are produced by subjection to high temperatures.

Ceramic quad flatpack (CQFP): An aluminum ceramic integrated circuit package with four sets of leads extending from the sides and parallel to the base.

CERDIP: A dual in-line package composed of a ceramic header and lid, a stamped metal lead frame, and frit glass to secure the structure.

Cerpack: A flatpack composed of a ceramic base and lid, a stamped metal lead frame, and frit glass to secure the structure.

Cerquad: A ceramic equivalent of plastic leaded chip carriers, consisting of a glass-sealed ceramic package with J-leads and ultraviolet window capability.

Chip: The individual circuit or component of a silicon wafer, also known as a die.

Chip carrier: An integrated circuit package, usually square, with a chip cavity in the center. Its connections are normally on all four sides.

Circuit: The interconnection of a number of components in one or more closed paths to perform a desired electrical or electronic function.

C-mode scanning acoustic microscope (CSAM): An analytical tool for the nondestructive evaluation of microelectronic packages via acoustic waves.

Coefficient of linear thermal expansion (CTE): The change in linear dimension per degree change in temperature, usually expressed as parts per million per degree Celsius.

Complementary metal-oxide semiconductor (CMOS): Logic in which cascaded field-effect transistors of opposite polarity are used to minimize power consumption.

Component: An individual functional element in a physically independent body that cannot be further reduced or divided without destroying its stated function. Examples include resistors, capacitors, diodes, and transistors.

Component lead: The solid or stranded wire or formed conductor that extends from a component and serves as a mechanical or electrical connection, or both.

Component lead hole: A hole used for the attachment and electrical connection of a component termination, including pins and wires, to a PC board.

Conductance: A measure of the ability of a material to conduct an electrical current.

Conductivity, electrical: The capability of a material to carry an electrical current.

Conformal coating: An insulative coating that conforms to the configuration of the object being coated.

Connector: Generally, all devices used to provide rapid connect/disconnect service for electrical cable and wire terminations, board to board.

Convection: A conveying or transference of heat or electricity by moving particles of matter.

D

Dambar: A portion of the lead frame that prevents mold compound from flowing to the ends of the lead frame.

Design of experiments: A systematic methodology for planning an experiment in order to consider all input and output variables.

Dicing: The separation of a semiconductor wafer into individual dies.

Die: The individual semiconductor element or integrated circuit, also known as a chip.

Die bonding: The attachment of an integrated circuit chip to a substrate or header.

Die paddle: The central portion of the lead frame, onto which the die and adhesive are placed during die attach.

Discrete: A term applied to single-element electrical components.

Dual in-line package (DIP): A component that terminates in two straight, parallel rows of pins or lead wires.

E

EIA: Electronic Industries Association.

EIAJ: Electronic Industries Association of Japan.

Electrode: A conductor through which a current enters or leaves an electrolytic cell.

Electronic packaging: The technical discipline of designing a protective enclosure for an electronic circuit so that it will both survive and perform effectively under a variety of environmental conditions.

Electrostatic discharge (ESD): The instantaneous transfer of charges accumulated on a non-conductor to a conductor, into ground.

Encapsulate: To seal or cover an element or circuit for mechanical and environmental protection.

Energy-dispersive X-ray (EDX) analysis: Normally, using electron beam excitation in the scanning electron beam microscope.

Eutectic: The minimum melting point of a combination of two or more metals.

External leads: Electronic package conductors for input and output signals, power, and ground.

F

Facedown bonding: A method of attaching a component or circuit chip to a substrate by inverting the chip and bonding chip contacts to the mirror-image contact points on the substrate.

Failure mode: Failure at the macro level, i.e., the observed effect of failure.

Farad: A unit of electric capacity.

Flatpack: An integrated circuit package whose leads extend from the sides and are parallel to the base.

Flip-chip: A chip that has bumped termination spaced on the face of the device and is designed for facedown mounting.

Footprint: The area occupied on a substrate by a component or element.

Frequency: Of an electric current, the number of hertz, or completed alternations per second.

Frit: A relatively low softening point of glass composition.

G

Gate array: A semicustom product, implemented from a fully diffused or ion-implanted semiconductor wafer carrying a matrix of identical primary cells arranged into columns with routing channels between them in x and y directions.

Ground: A common reference point for circuit returns, shielding, or heat sinking.

H

Hermetic: Sealed so that an object is gas-tight, to a specific rate, normally less than 1×10^{-6} cc/sec of helium.

High-density plastic quad flatpack (HD-PQFP): A package with greater than 196 leads and a pitch of 0.4 mm.

Hot dip: The process of covering a surface by dipping it into a molten bath of coating material.

I

I-lead: A surface mount device lead whose ends contact the board at a 90° angle; also called a butt joint.

Imidization: The reaction comprises acylation of the diamine with dianhydride in a polar solvent to give poly(amic acid), conversion of polyamic acid to polyimide with subsequent loss of small molecules, such as water.

Inductance: The resistance of an electric circuit to any change of current during the building up or decaying of a self-induced magnetic field. This property introduces a delay in current change, with resulting operational delay.

Infrared (IR): Radiant energy that is characterized by wavelengths longer than visible red (0.78 to $100 \mu\text{m}$ or 0.030 to 3.9 mils).

Input/output (I/O) terminal: A chip or package connector that interconnects the chip to the package, or one package level to the physically adjacent level in the hierarchy.

Insert: To assemble components, manually or automatically, into a PC board.

Insert cavity: A defined hole in the connector insert into which the contacts are inserted.

Insertion mount: The electrical and mechanical connection of a component to the surface of a conductive pattern utilizing component holes.

Insulators: A class of materials with high resistivity; materials that do not conduct electricity.

Integrated circuit (IC): A microcircuit consisting of multiple interconnected elements inseparably associated and formed on or within a single substrate to perform an electronic circuit function.

Integrated circuit chip: The active semiconductor element that is the functional part of the integrated circuit.

Intermetallic compound (IMC): An intermediate phase—homogeneous phase whose composition range does not include any pure metal—in an alloy system that has a narrow range of composition, but has an atomic bonding that can be of several types.

J

JEDEC: Joint Electronic Device Engineering Council.

J-lead: A surface mount device whose leads are formed into a “J” pattern, folding under the device body.

K

Kirkendall voiding: The formation of voids as a result of a disproportional diffusion rate between two neighboring materials.

Kovar: An alloy of 53% iron, 17% cobalt, 29% nickel, and trace elements, with a thermal expansion matching alumina ceramics and sealing glasses.

L

Laminate: A product made by bonding two or more layers together, usually of different materials, under heat and pressure to form a single structure.

Land grid array (LGA): The land grid array is a laminated ceramic multilayer package similar to a pin grid array, but without pins. The LGA uses gold-plated “landing pads” on 50-mil pitch similar to a leadless chip carrier (LCC), but in an array form. There are no leads, bumps, or solder. The package follows the existing laminated ceramic package manufacturing and assembly flows. The package length and width follow existing pin grid array outlines.

Large-scale integration (LSI): Usually, monolithic digital integrated circuits with a complexity of 100 or more gates or gate-equivalent circuits.

Laser bonding: Effecting a metal-to-metal bond of two conductors by welding the two materials together with a laser beam as a heat source.

Lead: A conductive path, usually self-supporting; the portion of an electrical component that connects it to the outside world.

Lead (Pb): A soft, heavy metal used in solder compositions and other alloys.

Leaded chip carrier: A plastic or ceramic chip carrier with compliant leads for termination.

Leaded surface mounting: The surface mounting of components to a substrate by means of component leads and solder joints.

Lead frame: The metallic portion of the device package that completes the electrical connection path from the die or dies and from ancillary hybrid circuit elements to the outside world.

Leadless chip carrier (LCC): An integrated circuit package that allows surface mounting of components directly into the substrate by means of solder joints.

Lead wires: Wire conductors used for intraconnections requiring fine wires or for interconnections that include input/output.

M

Marking: A method of identifying packages with part numbers, manufacturer code, and other information.

Mobile dislocations: Atomic line defects in polycrystalline material.

Modulus of elasticity: The ratio of stress to strain in an elastic material.

Moisture barrier bag (MBB): A strong, three-ply bag that is electrostatic discharge (ESD)-safe and allows minimal moisture transmission. The bag is intended to protect enclosed devices from moisture exposure and should not be opened till the devices are ready for board mounting.

Mounting hole: A hole used for the mechanical mounting of a PC board or for the mechanical attachment of components to the board.

Multichip module: A module or package supporting several chips on a single package.

Multilayer molded package (MM): A PQFP with enhanced performance achieved by a pair of power and ground planes. These planes significantly reduce the power-ground capacitance, making the package ideal for high-speed device operation.

O

Ohm: A unit of electrical resistance.

P

Package: An enclosure for a single element, integrated circuit, or hybrid circuit. It provides hermetic or nonhermetic protection, determines the form factor, and serves as the first-level interconnection externally for the device by means of package terminals.

Pad: The metallized area on a substrate or on the face of an integrated circuit used for making electrical connections.

PAMM: Plastic Assembly Manufacturing Module.

Piezoresistive elements: Pressure-sensitive resistors.

Pin grid array (PGA): A square package with pins covering the entire bottom surface at a pitch of 0.1 in. or 0.05 in., perpendicular to the plane of the package.

Pitch: The nominal distance from center to center of adjacent conductors.

Plastic leaded chip carrier (PLCC): A package with J-leads on all sides.

Plating: Metallic deposit on a surface, formed either chemically or electrochemically.

PPE: Plastic Package Engineering.

PQFP: Plastic quad flatpack.

Printed circuit board: A board with printed-on components as well as point-to-point connections.

PSMC: Plastic surface mount component.

Q

Quad flatpacks (QFPs): A generic term for surface mount technology flat packages with leads on all four sides; commonly used to describe chip carrier-like devices with gull-wing formed leads. The lead pitch for QFPs is in metric. The packages have no corner bumpers.

R

Real estate: The surface area of an integrated circuit or substrate.

Reflow: A soldering process that uses solder paste preprinted in a pattern on the PC board and heats the devices in place to make connections.

Resistance: The property of an electric circuit that determines, for a given current, the rate at which electric current is converted into heat. The power converted can be calculated by multiplying the current squared by the resistance.

Resistivity: The ability of a material to resist the passage of electric current.

Resistor: A device that offers resistance to the flow of electric current in accordance with Ohm's law: $R = E/I$, where R = resistance, E = voltage, and I = current.

S

Scanning electron microscope (SEM): A microscope that makes use of a scanning beam of electrons to image detail less than 100 angstroms in size (surface only).

Shrink DIP: A package resembling a DIP, with a lead pitch of 0.07 in., used in applications requiring high mounting densities.

Single in-line module (SIM): A module to which external connection is made by a row of conductors along one side.

Single in-line package (SIP): A package with leads on a single side only.

Small outline with J-leads (SOJ): A small outline package with J-leads.

Small outline package (SOP): A package with two rows of narrowly spaced gull-wing leads.

Solderability: The property of a component lead to be wetted by molten solder under specified conditions.

Solder coat: A process used to apply solder to package leads directly from a molten solder bath.

Specific gravity: The ratio of the weight of a given volume of a substance to the weight of an equal volume of water; also known as relative density.

Surface mount technology (SMT): Electrical and mechanical connection of components to the surface of a conductive pattern without using component holes. Components mounted in this manner are known as **surface mount devices (SMDs)** or **surface mount components (SMCs)**.

T

Tape-automated bonding (TAB): A chip interconnect process that can be used as an alternative to wire bonding.

Tensile strength: The greatest longitudinal tensile-strength stress a substance can bear without tearing apart or rupturing.

Terminal: A metallic termination device used for making electrical connections.

Thermal expansion: The expansion of a material when subjected to a temperature change.

Thermosonic bonding: The bonding of wires to metal pads on an integrated circuit by means of heat and ultrasonic scrubbing of wire into the pad to create a metallurgical bond.

Through-hole mounting: The electrical connection of components to the surface of a conductive pattern using component holes.

Tin whisker: A hairlike, single crystal growth formed on the metal surface.

Thin small outline package (TSOP): A plastic, surface mount memory package that features 0.5 mm pitch gull-wing leads located on two sides of the package.

Transmission electron microscope (TEM): A microscope used to obtain high-resolution images with a transmitted electron beam by electron lens imaging rather than scanning.

U

Ultrasonic bond: A bond formed when a wire is pressed against a bonding pad and the pressing mechanism is ultrasonically vibrated at a high frequency above 10 kHz.

V

Vapor phase soldering (reflow): The technique for soldering reflow to form package interconnections. The energy produced by the condensation of an inert vapor is used to heat solder joints.

Visual index: A visible mark, chamber, notch, tab, or depression indicating the position of pin 1, used to determine the orientation of an integrated circuit.

W

Wave soldering: A process in which PC boards are brought in contact with the surface of continuously flowing and circulating solder.

WDX: Wave-length dispersive X-ray analysis.

Wire bond: A completed wire connection that includes all its constituents and provides electrical continuity between the semiconductor die and a terminal.

Z

Zigzag in-line package (ZIP): A variation of a single in-line package with a lead pitch of 0.05 in., whose leads are bent to alternate sides, forming two rows, each with a 0.1 in. pitch.



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Packaging

With continuing commitment to quality and customer service, Intel has developed this first edition of the Packaging handbook. Of particular interest to Intel's customers is the technical information about its integrated circuit packaging methods. In addition to providing detailed IC packaging process information, this handbook includes, in its entirety, the Packaging Outlines and Dimensions Guide. Thus, providing a vital tool to the creation of quality systems products.

The industry move towards surface mount technology, denser packages, printed wiring boards, and systems has magnified the customers' requirement for more detailed IC packaging information from their supplier. With this in mind, this publication consolidates all relevant data for the IC package user in one place.

This handbook describes in detail the process flows involved in manufacturing both plastic and ceramic packages; electrical, thermal and mechanical data by package family; shipping and handling information; and a thorough discussion of surface mount technology, handling and assembly information for surface mount components.